Question 7: Potential derogations marked for reconsideration – Analysis of alternatives and socio-economic analysis

- The confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7] contains the full text including the confidential parts. This file is contained in the zip-file which we upload as confidential attachment.

Executive summary

A) Potential derogation proposed in Annex XV report

Paragraph 5 of the proposed restriction entry text includes "**ee.[the semiconductor manufacturing process until 13.5 year after EiF]**" as a potential derogation for reconsideration after the consultation.

We strongly appeal to keep the above derogation for *at least* 13.5 years after EiF and for the sake of clarity to add the equipment used for semiconductor manufacturing, so a derogation could therefore be:

By way of derogation, paragraphs 1 and 2 shall not apply to:

- *The semiconductor manufacturing process and equipment used to produce semiconductors until 13.5 year after EiF. This derogation shall be reviewed and assessed by the commission no later than 13.5 years after EiF.*

B) Additional derogation proposed by comment submitter

To avoid discussions about what is part of "the semiconductor manufacturing process" and considering the scientific evaluation of fluoropolymers (evidence see chapter 2.1h below) we propose an *additional* derogation:

By way of derogation, paragraphs 1 and 2 shall not apply to:

- *Fluoropolymers and articles containing fluoropolymers*

We provide the following input (the sub-chapters are referenced with the letters a) to g) used in the description of question 6):

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0) Definition of Terms

We produce *semiconductor/MEMS-based sensors* (e.g., pressure and inertial sensors), *ASICs and Power-Devices in semiconductor packages*, which are typically assembled on Printed Circuit Boards (PCBs) for electronic circuits (e.g., Electronic Control Units for vehicles, or in consumer applications like smart watches or wearables), as well as *Power-Semiconductor Modules* which are directly assembled on a cooling unit for applications mainly focusing on the electrification of vehicles. Definition of terms:

- The "Semiconductor Manufacturing Process" is a manufacturing process producing, processing, or using wafers or chips which are based on a semiconductor material.
- "Advanced Semiconductor Packaging" is a "Semiconductor Manufacturing Process" (as it uses semiconductor wafers/chips; consistently it's also listed under the heading "Semiconductor Manufacturing" in Annex A, table A.49)

The "Semiconductor Manufacturing Process" does not include any substance remaining in the article/product (e.g., etch gases or photo resists leave no traces in the article/product).

1) Semiconductor Fab

1.0) Introduction

We would like to emphasize the importance of taking the consultation comments #4304 by SEMI (RCOM part 13), #4449 by ESIA (RCOM part 18) and #4543 by JEITA et al. (RCOM part 21) into consideration when deciding on a derogation for the Semiconductor Manufacturing Process. In addition, the papers published by SIA PFAS Consortium under https://www.semiconductors.org/pfas/ explain the background of the Semiconductor Manufacturing Process well. Because of this, we don't explain the context of each sub chapter in full, but rather focus on specific inputs which our company can contribute.
For more global background information, the document "Impact of a Potential PFAS Restriction on the Semiconductor Sector.pdf" from SEMI comment #4304 (RCOM part 13) is particularly recommended.

1.1) Specific information per use

1.1.1) Deep Reactive Ion Etching (DRIE)

Deep Reactive Ion Etching of Silicon (DRIE) with vertical sidewalls (German Patent, US Patent Patentnr. DE-4241045, #5,501,893, 1992), is the standard semiconductor process used to produce structures in semiconductor MEMS (Micro-Electro-Mechanical Systems). MEMS production is based on Si wafer as a base material. For surface micromachining of MEMS sensors, a stratification of semiconductor, metal and dielectric layers get deposited and etched on the Si substrate, to produce a 3-dimensional MEMS element.
For some other applications in bulk micromachining, the bulk Si itself gets etched e.g., to produce a Si membrane for a MEMS pressure sensor. To etch Si as the functional material of a MEMS element, the MEMS industry uses the key DRIE trench process plasma etch technology.

1.1.1a.) Annual tonnage, emissions, and type of PFAS

Besides the SF_6 etch gas, the important process gas for Si DRIE trench etching is C_4F_8.
The DRIE trench etch process alternates periodically and rapidly between SF_6 etch and C_4F_8 passivation with typically 1-10 sec cycle times.
C_4F_8 with its highly efficient passivation behavior for the sidewall protection, avoids an isotropic lateral etch attack by fluorine radicals of vertical trenches in Si.

Besides these gases, CF_4 plasma with its low passivation behavior is used as a pre-trench etch step for native cxide removal in order to avoid an undefined start of the subsequent trench in Si. An undefined trench start would cause inertial sensor stiction risks and therefore a complete failure under critical working conditions in the field.

As semiconductor MEMS are produced with semiconductor processes in semiconductor fabs, DRIE is considered a semiconductor manufacturing process. As those are marked as a potential derogation for reconsideration after the consultation, we provide our input here related to question 7.

Information on tonnage and emissions is given in the overarching chapter 1.2a for the two gases used by our complany for this process: CF_4 and C_4F_8.

1.1.1b.) Key functionalities provided by PFAS for the relevant use

DRIE trench etching of Si with vertical sidewalls is a key enabling process in MEMS technology (Laermer & Urban, Challenges, developments and applications of silicon deep reactive ion etching, 2003). A 3-dimensional trench with vertical sidewalls in Si is crucial e.g., for the large market of in-plane capacitively detecting inertial MEMS sensors via comb structures, where the capacitance change and therefore the sensitivity increases with the aspect ratio between the combs.

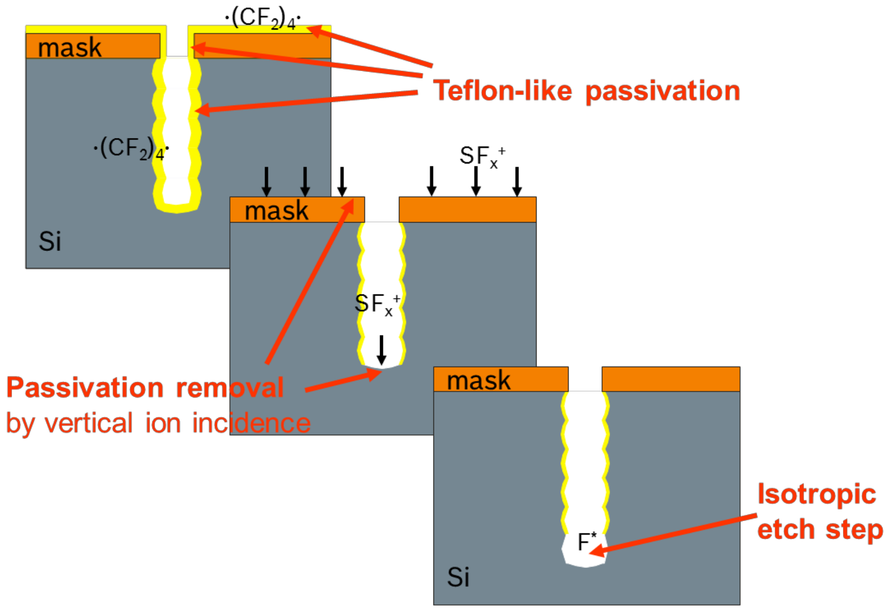

Figure 1.1.1b_1 Working principle of the "DRIE”" with subsequent C_4F_8 passivation and SF_6 etch steps with substrate biasing during an intermediate etch cycle to remove the passivation at the bottom of the trench by a vertical ion incidence.

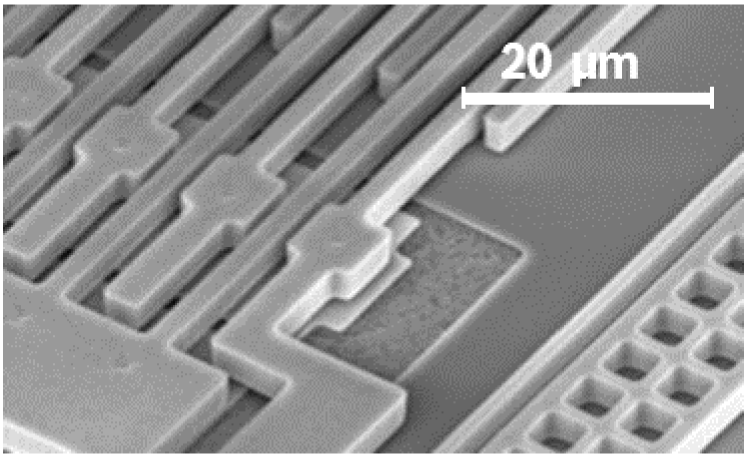

Figure 1.1.1b_2 SEM picture of a MEMS accelerometer comb structure.

Trenches with vertical sidewalls are also crucial for membrane type MEMS elements or through-the-wafer etches to achieve a high density of MEMS sensors and an efficient performance ratio on the wafer. Alternative methods such as wet-etching processes with KOH do not provide a crystal-orientated independent etching process, but instead provide 55° etch slopes to the 100-crystal plane, requiring significantly more silicon area (Laermer & Urban, 2019).

Without the highly efficient passivation behavior of C_4F_8 by providing a Teflon-like polymer deposition on the wafer, it wouldn't be possible to etch trenches in Si with vertical sidewalls at this high mask selectivity, where a simple resist mask can be used even for through-the-wafer etches (Chang, Leussink, Jensen, Hübner, & Jansen, 2017).

Therefore, and with its broad global use, C_4F_8 can be referred to as the key enabler for DRIE trench etching of Si (Chang, Leussink, Jensen, Hübner, & Jansen, 2017).

1.1.1d.) Alternatives

Alternative C_xF_y gases like CF_4, CHF_3, $C_2H_2F_2$, C_3F_8 have been evaluated with respect to DRIE trench etch passivation suitability in the past (Rhee, et al., 2008) (Rhee, et al., 2009), (Jansen, Boer, Unnikrishnan, Louwerse, & Elwenspoek, 2009).
Nonetheless, C_4F_8 with its strongly deformed ring molecule provided the highest passivation efficiency so far (Rhee, et al., 2008) (Rhee, et al., 2009) (Jansen, Boer, Unnikrishnan, Louwerse, & Elwenspoek, 2009).
The more efficient the passivation, meaning the lower time required in the deposition step of a process cycle for getting a dense passivation layer on the Si sidewalls, the faster the switching is possible between etch and passivation and the shorter the passivation steps can be chosen. Consequently, the production of wafers per hour increases with passivation efficiency under production conditions.

Besides development efforts for a replacement of C_4F_8 under DRIE trench process conditions, alternative non-trench-process DRIE etch processes could be enforced like e.g.:

- Plasma processes with SF_6/O_2 in a mixture, possibly adding HBr, Cl_2, SiF_4, where the anisotropy of the Si trench is achieved by the formation of SiO_2 as a Si sidewall protection (Jansen, et al., 2010).
- Cryogenic SF_6 plasma etching, where the anisotropy of a trench in Si is achieved by "freezing" the sidewall reaction below -120°C, in order to go below the activation energy necessary for the chemical reaction between Si and fluorine radicals Si + 4 F* -> SiF4 (Jansen, Boer, Unnikrishnan, Louwerse, & Elwenspoek, 2009), (Walker, 2001).

None of these processes have shown wide industrial implementation compared to the DRIE process with C_4F_8, due to the above mentioned reasons. In summary, there are two main and major advantages of the DRIE process we use compared to these alternative non-Trench-Process DRIE etch processes:

(i) the relatively large process window with respect to micro-masking, which enables high aspect ratio trenches and through-the-wafer etches, and

(ii) the high mask selectivity compared to other plasma etch processes.

This is due to the technique of alternating etch and deposition steps, where the passivation protects not only the Si sidewalls, but also the mask. This enables high aspect ratio trenches and through-the-wafer etches even with cheap resist masks under production conditions.

Besides this strong economic efficiency, resist masks also provide a performance factor especially for inertial sensor trenches, as feature accuracy and Critical Dimension loss variation across the wafer multiply through lithography and hard mask etch.

1.1.1e.) Status of R&D processes for finding suitable alternatives

Common for the **non-Trench-Process** DRIE etch processes is the relatively small process window between the regimes of micro-masking either due to an insufficient oxide removal at the bottom of the trench or due to “condensation” effects of the reaction by-products under cryo-conditions. Also common are difficulties with resist masks, where the resist mask selectivity would be low under mixed gas process conditions, together with a high risk of resist mask embrittlement under cryo-conditions (Jansen, et al., 2010) (Walker, 2001).

Alternative **non-PFAS** passivation gases for DRIE trench etching have been tested in the past, resulting in the finding that C_4F_8 with its strongly deformed ring molecule provided the highest passivation efficiency so far (Rhee, et al., 2008) (Rhee, et al., 2009) (Jansen, Boer, Unnikrishnan, Louwerse, & Elwenspoek, 2009).

Additionally, compared to the very high mask selectivity of the trench process, where even through-the-wafer etches can be realized with resist mask, these alternative non-Trench-Process DRIE processes would require hard masks especially for deep trenches, resulting in an increase of production costs for MEMS devices (Jansen, et al., 2010) (Walker, 2001).

1.1.1f.) Substitution timeline (technically and economically feasible)

Searching for alternative **non-PFAS** passivation gases for DRIE trench etching is expected to require an extensive evaluation program, if successful. After that a process adjustment and re-qualification for *each MEMS sensor design* (!) would be necessary. Because of the massive interaction of physical effects in MEMS sensor products this would even expand to re-qualifications on sensor product level where even a 13.5 year derogation could not be enough time to do so.

1.1.2) Deposition of Anti-adhesive coatings (reference to question 8)

Detailed information on the use of anti-adhesive coatings is given in detail in question 8, as part of it remains in the semiconductor MEMS and this ‘part’ is not covered by "the semiconductor manufacturing process".
As MEMS are produced with semiconductor processes in semiconductor fabs, the deposition of anti-adhesive coatings too is a semiconductor manufacturing process. As the semiconductor manufacturing process is mentioned for a potential derogation for reconsideration after the consultation, we also briefly mention the deposition of anti-adhesive coatings here in question 7 for completeness.

1.1.3) Plasma-enhanced chemical vapor deposition (PECVD)

Plasma-enhanced chemical vapor deposition (PECVD) is a chemical vapor deposition process used to deposit thin films from a gas state (vapor) to a semiconductor wafer. The chemical reactions involved in the process occur after creation of a plasma of the reacting gases. The

PECVD is often used to deposit films onto wafers containing metal layers or other temperature-sensitive structures. Beside the deposition of thin films, plasma etching processes are often also used on semiconductor equipment.

1.1.3a.) Annual tonnage, emissions, and type of PFAS

C_3F_8 is used in the PECVD process to remove silicon-oxide residuals from the chamber-walls (Kim, Oh, Lee, & Yeom, 2003). To etch SpinOnGlass- and Silicon Oxide-layers on these PECVD-tools,a mixture of CF_4 and CHF_3 is used.

Information on tonnage and emissions is given in the overarching chapter 1.2a for the PFAS gases used by our company for this process: C_3F_8 and CF_4.

1.1.3b.) Key functionalities provided by PFAS for the relevant use

The regular cleaning of the chamber is important to maintain the performance of the PECVD - equipment. The C_3F_8 is used to generate F-radicals in a plasma which subsequently will remove residues on chamber walls. In more modern PECVD tools, cleaning using NF_3 is the standard as the generation of F-radicals works more efficiently.

In the planarization process, the ratio of CHF_3 to CF_4 is important to adjust selectivity at the etching step. These compounds are known to have a slightly different selectivity (Zhang & Watson, 2019).

1.1.3d.) Alternatives

For chamber cleaning with C_3F_8, the use of NF_3 is an available alternative. The disadvantage of NF3 is that this compound is also a greenhouse gas, with a global warming potential (GWP) 16100 times greater than that of CO_2 when compared over a 100-year period. The GWP of C_3F_8 is calculated at 8900 (Myhre, et al., 2013).

The etching of silicon oxide films using F_2/Ar with a remote plasma (Kang, et al., 2007), the remote plasma etching of silicon nitride and silicon dioxide using NF_3/O_2 gas mixtures (Kastenmeier, Matsuo, Oehrlein, & Langan, 1998) and the cyclic etching of silicon oxide using NF_3/H_2 remote plasma and NH_3 gas flow (Gill, et al., 2021) are examples of alternatives which are being studied.
The mixture of CF_4 and CHF_3 is part of a very sensitive process of etching. For this process, it is currently not possible to determine when (and if at all) a non-PFAS alternative can fulfil the use-specific performance requirements of etching chemicals.

1.1.3e.) Status of R&D processes for finding suitable alternatives

Regarding the C_3F_8 the alternatively used NF_3 is already common and feasible. Still the conversion will result in notable increase in the production costs.

CF_4/CHF_3-Mixture:
Many studies have been conducted, but it is still not clear if non-PFAS alternatives will ever be available (Kastenmeier, Matsuo, Oehrlein, & Langan, 1998).
However, it should be possible to reduce the share of PFAS (especially CF_4) emitted to the environment by an optimized post-treatment of the exhaust gases (Krug, et al., 2022) (Fthenakis, 2001).

1.1.3f.) Substitution timeline (technically and economically feasible)

The switch from the chamber clean with C_3F_8 to the usage of NF_3 would take approximately 3-5 years, as the process requires a modification in the construction of the tool.

Searching for alternative non-PFAS etch gases to CF_4 and CHF_3 is expected to require an evaluation program for a period of at least 5 years.

1.1.4) Photolithography

The lithography process creates a photoresist mask defining the microchip's structures on the silicon wafer. It consists of the three sub-processes: (i) coating with photoresist, (ii) exposure of the resist under a chrome mask, (iii) developing. A photoresist has several specific parameters such as viscosity and photo speed which depend on the photoresist's ingredients. Photoacid generators (PAG) are needed in the lithography process to generate fine structures. The result of the lithography process is a resist mask with lines and spaces and their critical dimension (CD). To achieve the required CD at a high quality, it is substantial that the image can be transferred into the resist correctly. The fundamentals of optics need to be taken into account. To enable patterning of fine structures below 250 nanometers chemically amplified resists (CAR) are necessary. The chemical amplification, i.e., generating super-acidity, is mostly enabled by PFAS. This allows for an exposure process at a lower dose, enabling a better resolution of narrow structures.
PFAS are not used as a main process component in lithography but are essential additives to the photochemicals. Hence, PFAS occur as traces or residues in the lithography process. However, the PFAS additives play a substantial role for the lithography process.

The scaling criteria of step and repeat lithography are given by the Rayleigh equation, predicting the smallest optically definable image

$$R = k\frac{\lambda}{NA} = k\frac{\lambda}{n \sin\theta}$$

where
λ is the source wave length
n the medium refractive index
$n \sin\theta$ the numerical aperture (NA) with the incidence angle (θ)
k is a process dependent parameter

The smallest optically definable image – the optical resolution – is given by the fundamentals of optics. However, the photoresists characteristics, i.e., its ability to replicate the mask features is of critical importance (Knight, et al., 2010). In addition, the line-width variations (LWR) and line-edge roughness (LER) may impact device performance. Hence, the photoresist material's chemistry plays an important role. The transfer of the image of the mask onto the wafer surface is the most critical step of the semiconductor manufacturing process. If the image is not transferred correctly into the resist, no subsequent chemical or physical process can correct it (PFAS-Consortium of the Semiconductor Industry Association (SIA), 2023).

1.1.4a.) Annual tonnage, emissions, and type of PFAS

Many thousand liters of photoresist are processed in our company. PFAS may be used as additives to photoresist chemicals in lithography, underlying the intellectual property (IP) of the chemical supplier. The typical amount of PFAS in a resist is in the range of 0.01%.
An extract of typical photoresists and their PFAS content as well as liters used and the small PFAS portion of it can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].

Depending on the chips design, one part of the resist is solved in the developer and the other part remains on the wafer for patterning. After the lithography process, the resist mask is removed by plasma ashing.
The after treatment of PFAS resulting from lithography is threefold:

a) photoresist and thinner, which are not photo-processed
b) developer solution with resist residues
c) the resist mask after the patterning

a) The photoresist mixed with thinner is collected as organic waste solvent and then treated in a distillation process by a certified external specialist company.

b) There are residues of photoresist solved in the developer solution. This wastewater is neutralized and then fed into the municipal wastewater. An estimate of the extremly low concentrion of PFAS can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].

c) The resist mask after the patterning is plasma-ashed with oxygen plasma at high temperatures which leads to a destruction of the PFAS. >99.9% of PFAS in the plasma-ashing process is **not** released to the environment**.**

The total PFAS emission of the lithography process can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].

1.1.4b.) Key functionalities provided by PFAS for the relevant use

It is generally known that PFAS may be used as additives to optimize the lithography chemicals characteristics subject to the intellectual property (IP) of the photochemical supplier. PFAS are a substantial component of several resists, especially PAG.
Besides, there are process steps to treat the surface of the wafer, to improve the resist's adhesion and anti-reflective coatings to further enhance the exposure process (PFAS-Consortium of the Semiconductor Industry Association (SIA), 2023).
Today, the usage of chemically amplified (CA) photoresist is a standard in lithography to meet the process requirements. The CA-resists (CAR) allow for a process featuring low exposure doses to achieve the requested critical dimension (CD) and uniformity of the resist lines. CAR is a mixture of acid-sensitive polymers and photoacid generators. Base quenchers are added to limit the reaction and diffusion of the photoacid-catalyst into the unexposed regions in the photoresist film (Gaines, 2022) (Knight, et al., 2010).
In many applications fluorinated polyimides are applied on integrated circuits as an insulator and a buffer coater in the packaging. Important characteristics of the fluorinated polyimides coatings are moisture resistance, thermal stability, low dielectric constant and strong mechanical properties (high Youngs modulus, good fracture toughness).
Hence, PFAS play an important role in improving the polyimides' features (Ober, Käfer, & Deng, 2022).

1.1.4d.) Alternatives

PFAS are used as various additives in photochemicals. Research is focusing on finding alternatives. However, while certain PFAS-free material alternatives may be probable after more than 25 years of development, PFAS-free materials have not been proved to be viable or effective for the vast majority of photolithography applications. In specific cases like the PAGs, PFAS are required to enable super-acidity to achieve the required resolution of the pattern. A PFAS-free alternative has not been proven effective so far (PFAS-Consortium of the Semiconductor Industry Association (SIA), 2023) (Ober, Käfer, & Deng, 2022) (Knight, et al., 2010).

1.1.4e.) Status of R&D processes for finding suitable alternatives

PFAS are used as an additive to photo chemicals. These are the foundations of the IP of the photochemical suppliers. Research aims at finding alternatives to PFAS (PFAS-Consortium of the Semiconductor Industry Association (SIA), 2023). However, without the catalysts provided by PFAS, super-acidity may not be achievable. This is a subject of experimental studies. According to Ober et. al several alternatives to PFAS containing chemicals in lithography are under investigation (Ober, Käfer, & Deng, 2022) (Knight, et al., 2010)
Alternatives to current PAGs other than iodonium and sulfonium units as well as those that do not contain traditional PFAS have been studied. For the use in a CAR photoresist, the resulting acid must be as acidic as a perfluorosulfonic acid on the one hand. On the other hand, it needs to lack volatility so that it does not evaporate during the Post Exposure Bake (PEB), i.e. the bake step after the exposure and in the next generation photoresists possess minimum diffusivity (to enable high-resolution pattern formation) (Ober, Käfer, & Deng, 2022).

Recent patents have appeared that describe a number of related chemical structures, the goal of which is intended to deliver strong PAG performance and minimize the size of the fluorinated unit in the fluorosulfonic acid or eliminate it entirely. These new chemical structures will have to be assessed in terms of their viability as alternative PAGs as well as their performance characteristics (sensitivity, acid strength, and diffusivity) and environmental characteristics (fluorine content, degradation products, and toxicity) (Ober, Käfer, & Deng, 2022).

1.1.4f.) Substitution timeline (technically and economically feasible)

Qualifying new materials within the semiconductor manufacturing process is very complex. Today's semiconductor manufacturing processes consist of several mask layers comprising several hundred process steps. This leads to very complex systems with a multitude of sub-systems. A particular chemistry is designed to interact with other chemistries at each step of the semiconductor manufacturing process.

For numerous applications, PFAS-free alternatives would need complete reinvention. Academic research, material supplier research and development (validation), and scale-up are all part of the process of developing and implementing alternatives, which is then followed by device manufacturer efforts toward demonstration (verification), integration and implementation, and scale-up to high volume mass production.

For a PAG component change, multivariable evaluations on both the chemical supplier (verification) and semiconductor device manufacturer (validation) sides are required to prove that the change will not detrimentally impact the photoresist product. As a result, each product being replaced requires extensive research and development to confirm that critical functional requirements are acceptable.

Although each PFAS use presents distinct challenges and development timelines, most lithographic applications are likely to take 15 to more than 20 years to develop and approve a PFAS-free alternative, with the exception of PAGs, which are expected to take more than 25 years.

Needless to say, potential alternatives must be evaluated on a case-by-case basis, taking into account both technological (as mentioned above) and economic factors. To replace all PFOS and PFOA materials for example, an estimation of cost of these qualifications of an average of $60 million USD per semiconductor device manufacturer was calculated (PFAS-Consortium of the Semiconductor Industry Association (SIA), 2023) (Ober, Käfer, & Deng, 2022).

1.1.5) Oxide etch

The Plasma etching of silicon oxide layers is an important process in MEMS and the semiconductor industry.
The process-relevant, specific fluorine-containing gases are ionized in the plasma, with which the silicon oxide layer is then etched.

1.1.5a.) Annual tonnage, emissions, and type of PFAS

CF_4 (tetrafluoromethane) needed for silicon oxide etch, C_5F_8 (octafluorocyclopentene), C_4F_8 (octafluorocyclobutane) and mixtures thereof are needed for oxide etching with finer structures and/or smoother sidewall formation.
The different polymerization behaviors of the gases are essential.

Information on tonnage and emissions is given in the overarching chapter 1.2a for PFAS gases used by our company for this process: CF_4, C_5F_8, and C_4F_8.

1.1.5b.) Key functionalities provided by PFAS for the relevant use

The etching of SiO_2-layers happens in the fabrication of MEMS and semiconductor devices at many different stages during their path of production, each with specific requirements. In general, the PFAS act as F-radical source where CF_4 and C_4F_8 are considered less toxic than NF_3 and therefore easier to handle.
PFAS type CxFy etch gases enable the formation of gaseous SiF_4 from silicon and gaseous CO_2 from oxygen. Variable mixtures of the mentioned etch gases allow to:

a) tune required selectivity and to adjust etch profiles in anisotropic etch processes (etch rate in z-direction vs. x-/y-direction)
b) tune etch depth uniformity between areas with high and low feature density of an integrated circuit product
c) protect sensitive structures e.g., conducting paths

1.1.5d.) Alternatives

The usage of CH_4/SF_6 plasma (Man, Bao, Hao, Feng, & Ma, 2020), remote plasma etching of silicon nitride and silicon dioxide using NF_3/O_2 gas mixtures (Kastenmeier, Matsuo, Oehrlein, & Langan, 1998) and cyclic etching of silicon oxide using NF_3/H_2 remote plasma and NH_3 gas flow (Gill, et al., 2021) are examples of investigations alternatives to the above-mentioned oxide etch gases. It must be noted, however, that one of the experiments has been carried out without coating (Kastenmeier, Matsuo, Oehrlein, & Langan, 1998) or only for isotropic etching (Gill, et al., 2021).
With the information currently available on alternatives, our company can assume that remote plasma alternatives are possibly only suitable for isotopic etching. The anisotropic component is, however, absolutely necessary for the structuring of semiconductors. Remote plasmas are not suitable for anistotropic etching as they will not result in the same quality of etching.

Based on our experience, using a plasma of PFAS gas(es) or a gas mixture containing PFAS gas(es), the appropriate combination of anisotropic/isotropic etching and protective layer formation can be obtained. These etching processes are critical steps in the manufacturing of semiconductor devices.

The alternatively used etch gases SF_6 and NF_3 are also critical in respect to their potential as greenhouse gas. At some stages in the process flow they are already in use but at many others they cannot be used as the requirements of the specific stage do not allow for the use of greenhouse gases. The use of these alternatives can therefore be considered a regrettable substitution.

1.1.5e.) Status of R&D processes for finding suitable alternatives

The C_xF_y compounds in use are thus far irreplaceable at least in the short and medium term. The literature mentioned above shows that there are approaches for the upcoming challenges in finding suitable alternatives but nothing that has the necessary maturity for industrial use yet.
However, current investigations aim at reducing the share of PFAS (especially CF_4) emitted to the environment by an optimized post-treatment of the exhaust gases (Krug, et al., 2022) (Fthenakis, 2001) .

1.1.5f.) Substitution timeline (technically and economically feasible)

Searching for alternative non-PFAS etch gases as alternative for CF_4, C_5F_8 and C_4F_8 is expected to require an evaluation program for a period of at least 5 years. The timeline expected to find suitable alternatives for oxide etching and to implement each solution is expected in our point of view to be at least 15 years. The identification and requalification of affected manufacturing processes is likely to take longer than the 13.5 years proposed derogation period for semiconductor manufacturing processes.

1.1.6) Chillers for etch tools

1.1.6a.) Annual tonnage, emissions and type of PFAS

Exact temperature control is needed for etching processes (see chapter 1.1.1 and 1.1.5) to achieve the necessary precision of the etching process at low temperature. PFAS-containing Galden (Perfluoropolyether), Novec (Hydrofluoroethers) and Opteon (Hydrofluoroalkenes) are thus used in chillers for etch tools.
Information on used quantities and emissions can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].

1.1.6b.) Key functionalities provided by PFAS for the relevant use

Reactive ion etch (RIE) (chapter 1.1.1 and 1.1.5) plasma processes need a tight control of temperature in the process chamber within maximal a 0.2K range. This is realized by balancing of electrical heating and cooling in the chiller sub tools of the etch equipment. PFAS type cooling liquids with varying molecular weights (polymeric chain length) can be tailored for these applications. The exact control of the temperature range can be achieved

by using different chain lengths of the polymer, meaning a different type of Galden is needed for different temperature ranges.
The most positive properties of mentioned PFAS liquids are:

- being not corrosive against the chiller hardware that results in low maintenance costs
- having a low dielectric constant material where the cooling liquid is stable against arcing and reflected power in RF plasma environment (low polarity liquid insulator)
- having low viscosity for energy saving operation
- resulting in decreased process aborts due to less reflected power faults
- resulting in process stability of the etch process due to exact temperature control
- resulting in increased uptime of the etching tool.

1.1.6d.) Alternatives

Possible alternative is the use of glycol / water mixtures (which is used in PECVD processes) but these mixtures have some serious disadvantages for etch processes e.g.:

- Possible corrosion of the chilling system due to the aggressiveness of DI-water
- Unstable etching plasma due to reflected power faults caused by the high polarity of the glycol/water mixture and corrosion of the chilling system. This causes a higher conductance of the mixture
- Increased amounts of process aborts followed by wafer scrap
- Worse temperature control during process compared to PFAS (no stable etch temperature possible therefore no controlled trench process for MEMS and other semiconductors with fine structures possible)
- Glycol/water chiller are mainly compressor chillers which are using greenhouse gases

Due to these disadvantages mentioned above, a PFAS like Galden instead of glycol/water mixtures were used as chillers for etch tools for the past decades.

1.1.6e.) Status of R&D processes for finding suitable alternatives

Hydrofluoroethers (HFE) and hydrofluoroolefines (HFO) e.g. Opteon, are alternatives to purely carbon-fluorine PFAS. Nonetheless, HFE and HFO are PFAS substances and therefore are subject to the restriction proposal.
In addition, there are already chillers on the market that use carbon dioxide as a refrigerant. However, on the equipment side, this is a different circuit designed for a cooling liquid with specific properties, not for carbondioxide gas.
Further alternatives could be silicone oil and mineral oil but both alternatives are highly flammable. Additionally the use of silicone oil is prohibited in semiconductor manufacturing due to lithography-related issues, e.g. loss of photo resist adhesion.

1.1.6f.) Substitution timeline (technically and economically feasible)

Finding alternatives for Galden is possible but the research must be coordinated between chiller and etch tool manufacturer. This is necessary to ensure the communication between the two components. The qualification of all products on the chiller/tool pair is absolutely necessary.

Information on possible timelines and costs can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].

1.1.7) Various materials in the semiconductor manufacturing process, including O-rings, seals and chemical and ultrapure water distribution systems

1.1.7a.) Annual tonnage, emissions, and type of PFAS

Fluorinated polymers from the PFAS group are frequently used in the facilities of a semiconductor production fab, in addition to their use as process chemicals, e.g., for storage tanks and chemical distribution systems. Typical polymers are PTFE (polytetrafluorethylene), PFA (perfluoro alkoxy polymer), PVDF (polyvinylidene fluoride) in high purity grade. They are applied to ultrapure water (UPW) and semiconductor grade chemicals with high purity with respect to trace metals, anions and organic contaminants.
Fab installation also includes O-rings and seals made from perfluorpolyethers (PFPE),PTFE, and perfluoroelastomers (FFKM) as well as chemical resistant grease to ensure vacuum tightness of tube connections of process chambers and in chemical distribution and UPW systems.
A further significant application of fluorinated polymers are wafer carriers used in wet chemical processing at room and elevated temperatures, respectively. By default, the respective tool suppliers release the material of the wafer carriers for the various process chemical mixtures. Practically, PFA, PVDF or PTFE are the materials of choice. These materials are used in hydrofluoric acid (HF)-containing batch and single wafer clean tools as well as process baths in electro and electroless metal plating applications.

The fluorinated polymer-based chemical distribution systems are installed during fab construction and remain unchanged during the life time of the fab. Emissions from polymer materials are not expected, according to our knowledge, to occur.
To reduce the tonnage of PFAS type polymers, in many cases fluoropolymers are only used as inner liner material which is in contact with ultrapure water or electronic grade chemicals. The majority of the related installations (e.g., tanks) can be made of cheaper polymers or stainless steel as long as they do not come into contact with ultrapure liquids.
The amount of fluoropolymers in our semiconductor wafer fab can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].
O-rings and seals are normally only exchanged in maintenance situations and disposed via controlled ways so as to mitigate environmental contamination.
Wafer carriers for wet chemical processing belong to the tool configuration and are normally not exchanged.

1.1.7b.) Key functionalities provided by PFAS for the relevant use

These materials are resistant against aggressive chemicals (acids, bases) and solvents and can be applied at room and elevated temperature, respectively. Their very smooth surface enables them to be used for thorough surface cleaning from trace metals. This is a prerequisite for handling semiconductor grade chemicals and ultrapure water.
Manufacturers of these chemicals are using the same materials. To ensure a closed

cleanliness chain from chemical production to usage in wafer fabs, PFAS-based fluoropolymers must be used in wafer fabs as well.
O-rings of fluoropolymers are free of additives and ensure cleanliness in flange connections of chemical and UPW distribution systems.
The chemical and thermal resistivity of the mentioned fluoropolymers is even more important for wet chemical processing as mixtures of chemicals can generate increased potential for chemical degradation compared to their separated components (e.g. hydrogen peroxide and sulfuric acid vs. the mixture of both forming a piranha solution or etching, commonly known as carioc acid).

1.1.7d.) Alternatives

SEMI (Semiconductor Equipment and Materials International) standard F057 does not recommend special polymer materials to be used in wafer fabs. So far, only the PFAS materials described provide heat and chemical resistance against semiconductor grade chemicals and ultrapure water.
When polymeric material is required for wafer handling, there are currently no known alternatives.
Quartz or fudes silica may be utilized as a wafer carrier in a chemical bath for wet chemical processing if the process chemistry permits it (acidic chemical mixtures without hydrofluoric acid, solvents).

1.1.7e.) Status of R&D processes for finding suitable alternatives

Using PFAS-based polymer materials is the outcome of long-term materials testing for semiconductor fab installation for chemicals and UPW. There are currently no known alternatives to PFAS-containing O-rings, seals and chemical and ultrapure water distribution systems which are used in the semiconductor manufacturing process.

1.1.7f.) Substitution timeline (technically and economically feasible)

A timeline to exchange installations of currently running wafer fabs cannot be proposed as this would require a fab shutdown and complete reconstruction.
Alternative materials for chemical and UPW distribution systems could be used, if available, only in newly planned semiconductor wafers fabs.

1.2) Overarching information

1.2a) Annual tonnage, emissions, and type of PFAS

None of the below listed PFAS remain in an article, but are rather pure process gases. All equipment is installed in conjunction with exhaust gas scrubbers working at >900°C. So typically, >99% (DRE, destruction removal efficiency) of

(i) PFAS process gases, their
(ii) crack products formed in the plasma, and the
(iii) volatile plasma etch reaction by-products in the exhaust of a plasma reactor

don’t enter the atmosphere. Instead, they get precipitated and trapped in a liquid phase in the exhaust scrubber systems which then is disposed of.

Values of annual usage and emissions can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].

1.2c) The number of companies affected

The whole industry with semiconductor and MEMS production facilities in Europe and equipment suppliers are affected. Non-European production facilities are not affected. This universal PFAS restriction proposal therefore poses an enormous competitive disadvantage for semiconductor manufacturers, like our company, based in regions where the PFAS restriction proposal falls compared to their non-affected competitors.

1.2g) Socio-economic impacts

Life cannot possibly be imagined without MEMS devices, as they penetrated our everyday life in IoT, medical, automotive and consumer applications. Due to semiconductor-based MEMS production technology, MEMS devices and sensors can be produced at low cost for the mass market compared to former precision mechanical elements.
On the one hand, MEMS sensors are vastly used in consumer electronics e.g., environmental sensing, motion sensing, micro speakers, altitude measurement for indoor navigation, image stabilization, image rotation and many more applications in consumer electronics mobile devices like fitness trackers or smartphones.
On the other hand, MEMS sensors are used by all modern automotive OEMs (original equipment manufacturers) in several automotive applications e.g., acceleration sensors for Airbag systems or inertial sensors for Electronic Stability Programs (ESP) in vehicles.

Taking this very broad use in account and when looking at the chapters "Alternatives" for the different uses above, one can clearly conclude that without a long and reasonable derogation time for the semiconductor manufacturing process there would be extremely detrimental socio-economic consequences on the semiconductor industry. Simply put, it would mean an even more severe drop in the worldwide production of smartphones, wearables, and cars than seen in the last years by the semiconductor supply crisis.

If one only looks on the above-mentioned process chemicals, which don't remain in the product, MEMS production could move outside Europe and this would lead to a significant loss of jobs, competitiveness and competence, destroying one of the few sectors in semiconductor industry in which European companies hold a leading position worldwide. (Yole Group, 2021)
Concerning the various fab equipment outlined in chapter 1.1.7: If PFAS-based fluoropolymer materials would be restricted within the EU in the near future, no new semiconductor wafer fabs could be constructed with the corresponding impact on the EU chips act. Doubling the semiconductor market share of the EU by 2030 would be impossible.

2) Advanced Semiconductor Packaging

2.1) Sintering of semiconductor chips to a heatsink

Semiconductor Power Modules are produced with semiconductor processes, using semiconductor materials. The following is related to the manufacturing process of Power-Semiconductor Modules – the sintering of a semiconductor chip to a heatsink – and is therefore covered by the definition of "Advanced Semiconductor Packaging". One PFAS plays a crucial role in this process.

It is currently not possible to demonstrate that a non-PFAS alternative can meet the application-specific performance requirements for the kinds of applications described below.

In this case, it may be necessary to discover novel chemicals and/or different ways to create Semiconductor Power Modules that provide the required performance. Invention is a never-ending process with no set deadline or guarantee of success. It is therefore necessary to (i) outline our specific applications that rely on PFAS materials for specific performance requirements, and (ii) highlight the need of exemptions or at least derogations for our specific uses of PFAS materials in Semiconductor Power Modules.

Within the electrified powertrain of battery electric vehicle (BEV) or plug-in hybrid electric vehicle (PHEV), the so-called power module switches the DC current from the battery to generate the AC current for the electrified motor. With every switching step, heat is generated within the power module. For this reason, the power modules need an active cooling – a connection to the cooling water circulation within the BEV or PHEV.

The base of the Power-Semiconductor module is a substrate – typically with high thermal-conductive ceramic materials, on which a semiconductor chip (e.g., Si-IGBT, or SiC-MOSFET) is applied. To enable high power over a long lifetime – a key for high-efficient power electronic applications -, the connection between substrate and semiconductor must provide high thermal and electrical conductivity. An effective material in use here is silver. A simple sketch of a power module is shown in *Figure 2.1_1*.

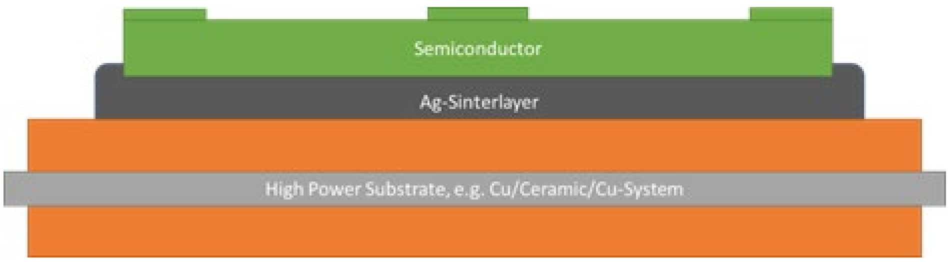

Figure 2.1_1: Simple sketch of a power module which might be used in an electromobility application.

The Power-Semiconductors can be considered as the heart of the inverter. To enable an as low as possible low resistance electrical connection, the semiconductor components are nowadays assembled by an Ag sintering process:
On the substrate, a sinter material, containing mostly of Ag particles in µm- or sub-µm-size, and the electrical component is applied. By applying pressure – up to 40 MPa and

Temperature – about 250 – 300°C, depending on the paste system, the sinter material is highly compressed, and a compact Ag material with a porosity of below 10% Vol.% is achieved. A major advantage of the sinter-process is that the silver-based properties such as thermal conductivity are also realized without melting. The sintering temperatures of < 300°C are therefore far below the melting point of silver, which is around 962 °C. This manufacturing process therefor allows to build high performance (thermal conductivity) interconnections without the high stress of a melting related connection or without exceeding limit temperatures of sensitive semiconductor components.
As described in figure 2.1_2 below it is not possible to perform the sintering without an additional layer between the semiconductor chip and the sinter tool I.

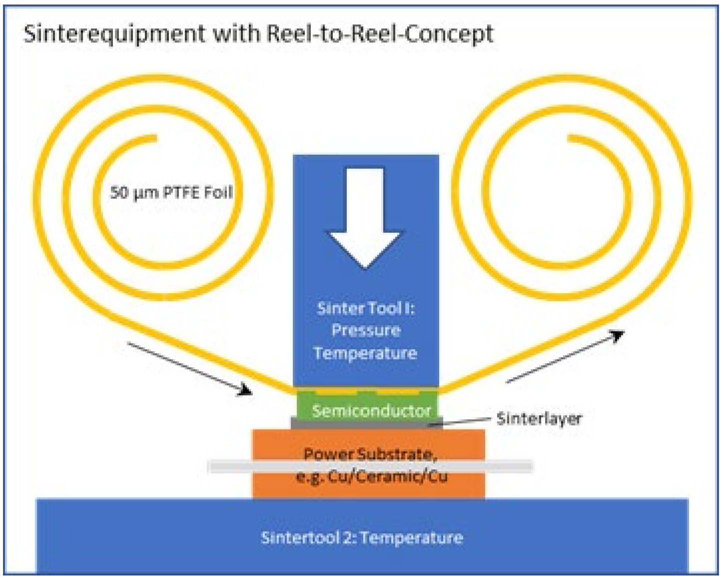

Figure 2.1_2: Sketch of a Sinter Equipment with PTFE-Reel-to-Reel-handling.

Solid film PTFE (typically 50 µm Foil) is used during sintering process with high pressure (~10 – 40 MPa) and high temperature (~250 – 300°C) as separator between semiconductor (Si, SiC, GaN, metal parts) and sinter tool (steel).

Functions of the separator foil:

- mechanical protection of semiconductor during process
- protection of semiconductor against contamination and particles from sinter tool
- no release of particles from the separator foil
- homogenization of pressure: compensation of topology (roughness) (gate runner/signal contacts, source pad)
- resistance/stability at process conditions (~ 280°C, 10 – 40 MPa, < 300 s)
- high releasability from semiconductor surfaces:
- no sticking
- no peeling of semiconductor structures (as isolator material, pad metallization)

An example picture of a Semiconductor Power Module can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].

2.1a.) Annual tonnage, emissions, and type of PFAS

This information can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].

2.1b.) Key functionalities provided by PFAS for the relevant use

PTFE as thin film (50 µm), used as separator within the sintering process provides the following key functionalities:

- mechanical protection of semiconductor
- protection of semiconductor against contamination and particles
- homogenization of pressure: compensation of topology (gate runner/signal contacts, source pad)
- resistance/stability at process conditions (~ 280°C, 10 – 40 MPa, < 300 s)
- high releasability from semiconductor surfaces:
    - no sticking
    - no peeling of semiconductor structures (as isolator material, pad metallization)

2.1c.) The number of companies affected

Our company has no information about this. All manufacturers of Power-Semiconductor Modules which are using this sintering process are affected.

2.1d.) Alternatives

Based on current research, discussion within the power electronics community, and feedback from material and equipment suppliers, no alternatives are available and foreseeable.

For PTFE during the sintering process no alternatives are available, based on the following information:

- public founded project ProPower (2015)
- tests within the development of a former Power-Semiconductor-Module (2018)
- discussion with equipment and material suppliers (2023).

Polymers with high temperature robustness as thermoplastic polyimide (PI) or polyetheretherketone (PEEK) do not offer all relevant and required parameters:

- mechanical homogeneity at high temperatures is not given
  → PEEK/PI do not creep to homogenize
- interaction with semiconductor surface critical (PI sticks to component)

For this reason, it is not possible to provide a reliable timeline for a possible new PFAS-free alternative for this specific manufacturing process.

2.1e.) Status of R&D processes for finding suitable alternatives

Typical timeline for the implementation of a new technology and process, new equipment in case alternatives would be available are:

- 3-5 years of research/predevelopment to identify alternatives and assess risks and interactions within electronic environment with special requirements because of high voltage applications
- 3-5 years for process development, new equipment set-up and release
- additional confirmation and qualification at customer to be clarified, if necessary, additional 2-3 years at the OEM (original equipment manufacturer).

Based on this theoretical estimation a timeline is between 8 and 13 years. The base requirement for this described timeline is a positive scouting of potential alternatives.
As mentioned above, PFAS-free alternatives for the manufacturing of Power-Semiconductor Modules are currently not available and not foreseeable in the near future.

2.1f.) Substitution timeline (technically and economically feasible)

For this reason, it is not possible to provide a reliable timeline for a possible new PFAS-free alternative for this specific manufacturing process.

2.1g.) Socio-economic impacts

This information can be found in the confidential attachment [01_Confidential_PFAS_Feedback_to_ECHA__Att_Question_7].

2.1h.) On fluoropolymers, proposed additional derogation

Above we described the use of PTFE, which is a fluoropolymer. Fluoropolymers meet the criteria of the OECD as a polymer of low concern (OECD, 2009):

- stable (“do not degrade in the environment”)
- large (“cannot enter human cells or trigger events within cells”)
- non-toxic (“safe to use from an environmental and human perspective”)
- non-bio accumulative (“cannot accumulate in the body”)
- low molecular weight (MW) leachable
- fulfilling limitations of reactive functional groups

The fluoropolymer materials show no environmental critical behavior beside the main property of “persistence” (Henry, Carlin, Hammerschmidt, Buck, & Buxton, 2018). For this reason, we propose a wide and timely unlimited derogation for fluoropolymers as stated in the executive summary:

By way of derogation, paragraphs 1 and 2 shall not apply to:

- *Fluoropolymers* (according to the definition of fluoropolymers of the OECD (OECD, 2021)) *and articles containing fluoropolymers*

If this is considered to be not adequate, because it's too broad or general we would suggest to rephrase our above proposal to this:

By way of derogation, paragraphs 1 and 2 shall not apply to:

- *Fluoropolymers for sintering of semiconductor chips to a heatsink*

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List of confidential attachments

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