PFAS-Containing Materials Used in Semiconductor Manufacturing Assembly Test Packaging and Substrate Processes

Semiconductor PFAS Consortium Assembly, Test, Packaging and Substrates Working Group

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This publication was developed by the Semiconductor PFAS Consortium assembly, test, packaging and substrates technical working group. The contents do not necessarily reflect the uses, views or stated policies of individual consortium members.

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About the Semiconductor PFAS Consortium

The Semiconductor PFAS Consortium is an international group of semiconductor industry stakeholders formed to collect the technical data needed to formulate an industry approach to perfluoroalkyl and polyfluoroalkyl substances (PFAS).

Consortium membership comprises semiconductor manufacturers and members of the supply chain including chemical, material and equipment suppliers. The consortium includes technical working groups, each focused on the:

- Identification of PFAS uses, why they are used, and the viability of alternatives.
- Application of the pollution prevention hierarchy to (where possible) reduce PFAS consumption or eliminate use, identify alternatives, and minimize and control emissions.
- Development of socioeconomic impact analysis data.
- Identification of research needs.

This data will better inform public policy and legislation regarding the semiconductor industry's use of PFAS and will focus R&D efforts. The Semiconductor PFAS Consortium is organized under the auspices of the Semiconductor Industry Association (SIA). For more information, see www.semiconductors.org.

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Executive Summary

The assembly, test, packaging and substrate (ATPS) portion of the semiconductor industry uses perfluoroalkyl and polyfluoroalkyl substances (PFAS). ATPS connects the integrated circuit die or chip to the outside world, such as a printed circuit board (PCB), and provides environmental and mechanical protection to the die and heat removal; without a package, the die may fail prematurely. As packaging becomes more and more complex due to decreasing die size, increased processing speed, and increased package complexity, the combination of properties required to meet these challenges are often only found in PFAS which are known to be thermally and chemically stable and provide electrical properties such as low dielectric constant and loss necessary for high-speed and high-bandwidth communication.

Within this paper, the PFAS Consortium identifies applications of PFAS within the ATPS processes and potential and replacement alternatives. Packaging materials interact with both the silicon die and the end product. Some of these interactions require extensive quality, reliability and other types of testing to ensure final product functionality. Given that the assembly process is an interaction between the fabrication plant and the end product, it is possible that there could be die and passivation materials from multiple fabrication plants, or multiple PCBs and second-level interconnect materials. This creates extensive complexity: a change in one assembly material could require testing across multiple silicon die or second-level interconnect vendors or the electronic customer incorporating the package into their final product.

Because of all of the possible interactions, changes to packaging materials where available could take anywhere from five to 15 years to implement. Changes to assembly package materials can also vary based on the complexity of the change in the material, as well as the extent of the interactions. The cost for each substitution will depend in part on package complexity (how many other materials the changed material interacts with) and package size. In addition, proof of the long-term performance of new materials in operational scenarios may take additional time.

This paper includes data collected through PFAS consortium surveys, as well as information representing the current state of knowledge regarding the use of PFAS in semiconductor packaging. Additionally, Pradeep Lall, Ph.D., M.B.A., a MacFarlane Endowed Distinguished Professor with the Department of Mechanical Engineering and Director of the NSF-CAVE3 Electronics Research Center at Auburn University, conducted packaging literature and patent reviews as well as interviews with packaging experts.

1.0 Introduction

In the semiconductor industry, a “package” refers not to the box in which the device is contained but to the combination of materials and structural elements that connect an integrated circuit (IC) to a printed circuit board (PCB), interposer or device, while protecting the package from environmental influences. The package allows the IC to be able to connect to other components on the PCB.

ATPS represents a broad range of materials, used across multiple process steps, requiring varying material properties and quality characteristics. Across this breadth, there are properties that stand out as essential such as thermal and chemical resistance, low dielectric constant, low residue transfer, improvement of wetting/spread, and the ability to reduce surface energy and photo-imageable functionality. These characteristics are required for necessary product performance, yield, quality and reliability, as well as enabling the multistep processing needed for the complex packages of the future.

The ATPS supply chain is highly complex with multiple layers of suppliers across multiple geographies. Because PFAS have not yet been regulated as a class, traceability for those compounds throughout the

entire ATPS supply chain is difficult and would require a multicompany, multistep, multiyear effort to improve the level of knowledge within the supply chain. Within this paper, the PFAS Consortium identifies known and potential applications of PFAS within ATPS processes and identifies potential replacement alternatives.

1.1 Objectives and Scope of This White Paper

Given evolving concerns regarding the persistence, bioaccumulation, mobility and toxicity of some PFAS, there are several efforts to develop regulatory restrictions that would limit the use of PFAS-containing materials to only those deemed essential to the functioning of society.

In this paper, we will focus our discussion of essential use as "necessary for highly important purposes in semiconductor manufacturing for which alternatives are not yet established" and apply the essential use concept described by Cousins et al. (Cousins et al. 2019) to show that these compounds should be considered essential for certain processes in semiconductor ATPS because they provide vital functions and are currently without established alternatives.

The objectives of this white paper are to identify the principal applications of PFAS-containing ATPS manufacturing materials, determine the application-specific performance requirements of PFAS uses in ATPS, and assess the role of fluorine vs. alternatives in fulfilling performance requirements.

To the extent that PFAS-containing materials are essential to ATPS manufacturing, we will describe the uses and unique properties of PFAS, which justify their current uses as required in semiconductor manufacturing and for which alternatives have not yet been adequately identified. To the extent that nonfluorinated alternatives may be available that can satisfy the application-specific performance requirements, we will describe the development and/or qualification parameters necessary to validate commercial viability. Where possible, we will also identify the potential avenues of research and development for new materials and potential releases or exposures of PFAS-containing ATPS materials.

1.2 PFAS-Containing Materials Used Within Semiconductor ATPS

There is no agreed-upon single, consistent definition for PFAS. A complicating factor is the lack of consensus for the term "PFAS" within the multitude of regulatory development activities. Since the purpose of this white paper is to document the use of all materials that could potentially meet a regulatory definition of PFAS, along with the performance requirements required to determine the criticality or essentiality of the use, the Semiconductor PFAS Consortium has defined the scope of materials described here to include all of chemistries and materials that contain molecules with $-CF_2-$ and/or $-CF_3$.

Packaging has evolved over the last 50 years or so from ceramic packages to organic packages. There have been significant material changes over that time, including the move to lead-free and halogen-free packaging. Packages have become increasingly complex as well: smaller and thinner packages to enable mobile devices and large, multichip modules with individual die(s) for computing, graphics, memory, Wi-Fi or other functionality. It is possible to stack dies and packages on top of each other, or to embed dies within the substrate.

Specific mechanical, electrical and thermal properties of an assembled package could drive various material property requirements. With semiconductor substrates trending toward miniaturization and high density, the resistance-capacitance (RC) delay now exceeds the transistor gate delay and becomes the limiting factor of the device performance (Martin, et al. 2000). Besides interconnect dimensions, the RC delay also depends on such material properties as metal resistivity and dielectric constants; specifically, the RC delay increases with an increasing dielectric constant and a decreasing thickness of the dielectrics used as substrate materials. Reducing the dielectric constants of substrate materials reduces the RC delay

and enables the use thinner dielectric materials, which is beneficial for device miniaturization. Designers can also expect reduced crosstalk and power dissipation when using substrate materials with low dielectric constants; therefore, substrate materials with low dielectric constants and losses are vital for high-speed and high-frequency applications.

Signal attenuation or insertion loss is one of the key aspects for a successful high-speed interconnect design. One component of the attenuation constant is dielectric loss caused by the polarization of substrate materials, which is exacerbated at the high frequencies needed for high-speed transmission. Another component of the attenuation constant is metal conductivity loss, to which one of the major contributors is the skin effect, defined as an increased current density at the conductor periphery surface as frequency increases (Lo and Cheah 2015).

In conventional packaging assembly processes, surfaces of the conductor (typically copper) and dielectric materials are often pre-treated and roughened to provide mechanical interlocks that enhance adhesion between two consecutive layers. The demand for low insertion loss drives efforts to reduce the surface roughness of the conductor and to develop solutions that improve adhesion between dielectric materials and a copper surface that's not rough, as there are minimal anchoring sites on a smooth copper surface for mechanical interlocks. Applying adhesive materials improves adhesion between dielectrics and smooth copper. An ideal adhesive for this application should share the same characteristics as core and buildup dielectrics, including a low dielectric constant.

Among all polymeric dielectrics, perfluoroaliphatic polymers have the lowest dielectric constants (1.9 to 2.1) and are widely used as substrate materials. PFAS-containing materials exhibit a unique combination of outstanding physical and chemical properties needed for applications in the semiconductor ATPS manufacturing processes, including high thermostability and chemical inertness to acids, bases and solvents, and low moisture absorption.

The use of PFAS-containing materials within semiconductor ATPS manufacturing processes plays an essential role in the success of advanced packaging technology. The benefits PFAS provide include low surface energy, low dielectric constant, low moisture absorption, low residue, and high thermal and chemical stability. The types of materials in semiconductor ATPS manufacturing include substrates, adhesives and processing aids. Some of the current challenges in advanced packaging include how to effectively maintain material surface energy and product performance, how to conduct processing with multiple thermal- or chemical-related steps, and how to improve signal strength and reliability.

There are three main structural elements in a package (see Figure 1):

- The package substrate, which:
  - Consists of interconnect layers (typically six to 24 layers in a processor package) to connect the IC chip to the PCB.
  - Uses high-density interconnect wiring vs. a motherboard PCB.
  - Contains redistribution layers to fan out or fan in the interconnects to the pitch required.
- The silicon die (or chip)-to-substrate connection, which:
  - Has a first-level interconnect (FLI) that typically includes solder bumps or microbumps, controlled collapse chip connection (C4) bumps or other types of connections.
- The substrate to the PCB, which:
  - Has second-level interconnect (SLI) that is typically solder balls called ball-grid array (BGA) or it could utilize other types of connections like lands, wires, etc. as shown in Figures 6-9 below.

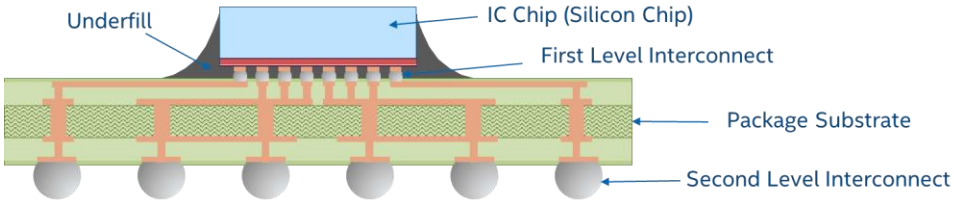


Figure 1: Structural element package diagram

As shown in Figure 2, there are numerous materials included in a package that have required properties for both functionality and to enable production. Properties can include thermal stability, the ability to flow, and the ability to stick (or not to stick in some cases).

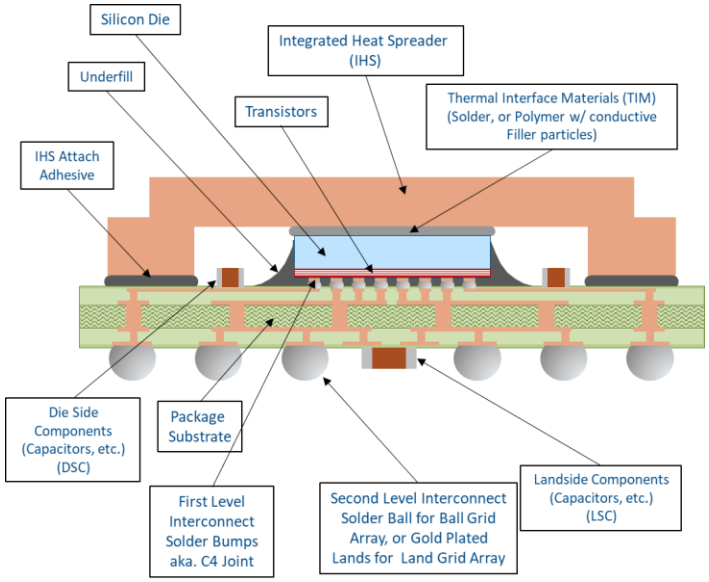


Figure 2: Material package diagram

The package has many important functions (see Figure 3), including mechanical protection, power delivery and heat removal.

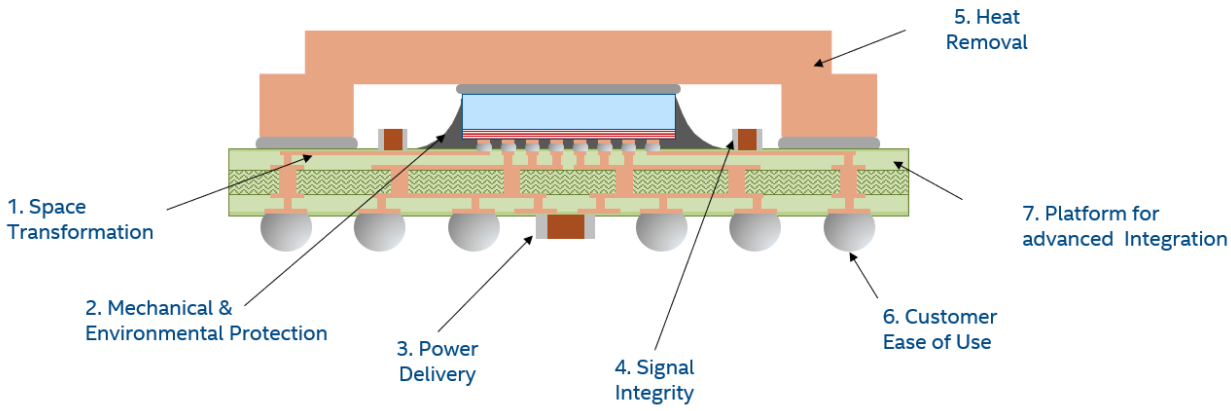


Figure 3: Functional package diagram

A microprocessor package substrate plays a critical role in connecting advanced transistors on silicon and improving computing functions. This substrate provides mechanical handling and protection for the smaller, fragile IC. Directly attaching silicon chips such as microprocessors to the motherboard would require both advanced PCB feature sizes and board assembly processes and materials technology, which would increase overall system costs.

Figure 4 illustrates the difference in pitch for the red, green and blue lines between a package and direct-chip attach. The substrates themselves (Figure 5) are layers of copper and organic materials to route signals from the die to the motherboard.

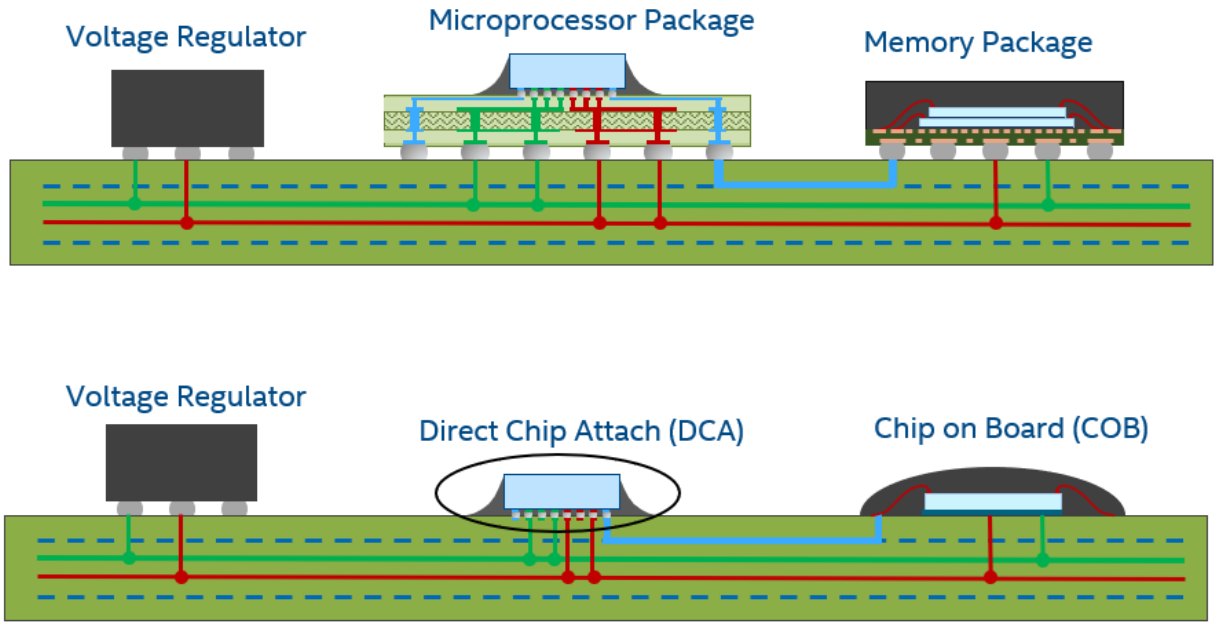


Figure 4: Multichip package diagram

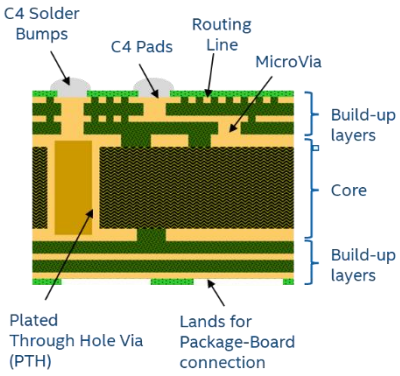


Figure 5: Substrate cross-section

Some basic chip-to-package interconnection types include wire bond and flip chip. It is possible to broadly characterize modern package types into two types:

- Organic substrate packaging. Its architectures include BGA, which may use wire-bond interconnects (as in a plastic BGA) or flip chip interconnects (as in a flip chip BGA).

- Leadframe packaging, which may be leaded or leadless. Leadframe packaging with leads include quad-flat pack, small outline IC and flip-chip small outline package. Leadframe packaging with no leads include quad-flat no-lead and small outline package.

Different package types usually require different materials, such as a mold for wire bond or an underfill for flip chip. Figures 6, 7 and 8 illustrate how packages differ based on functionality, cost, size, etc.

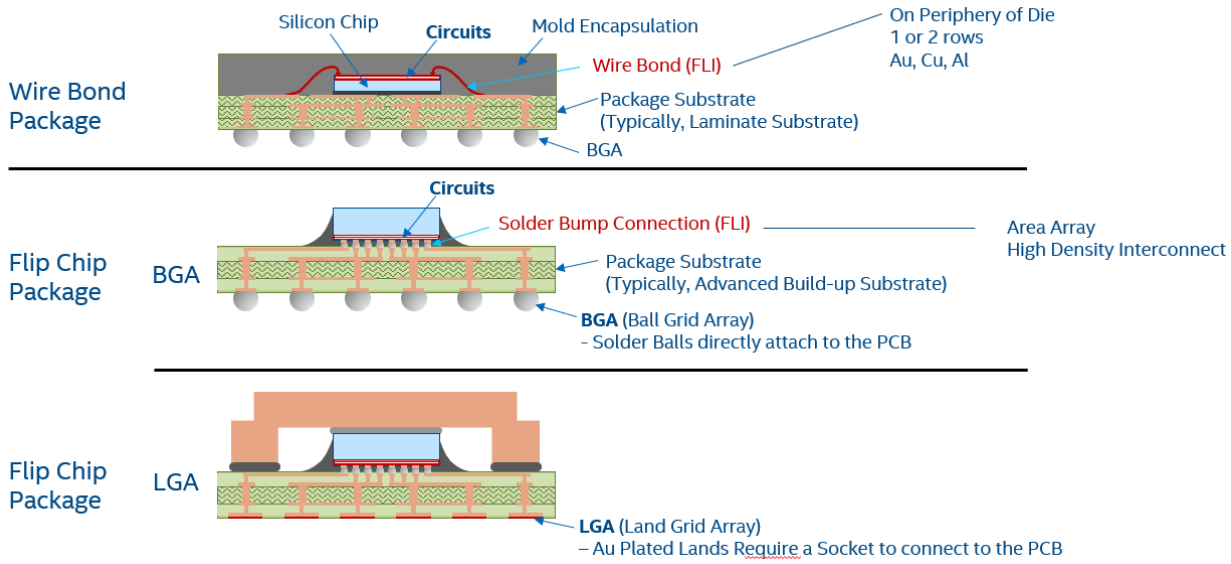
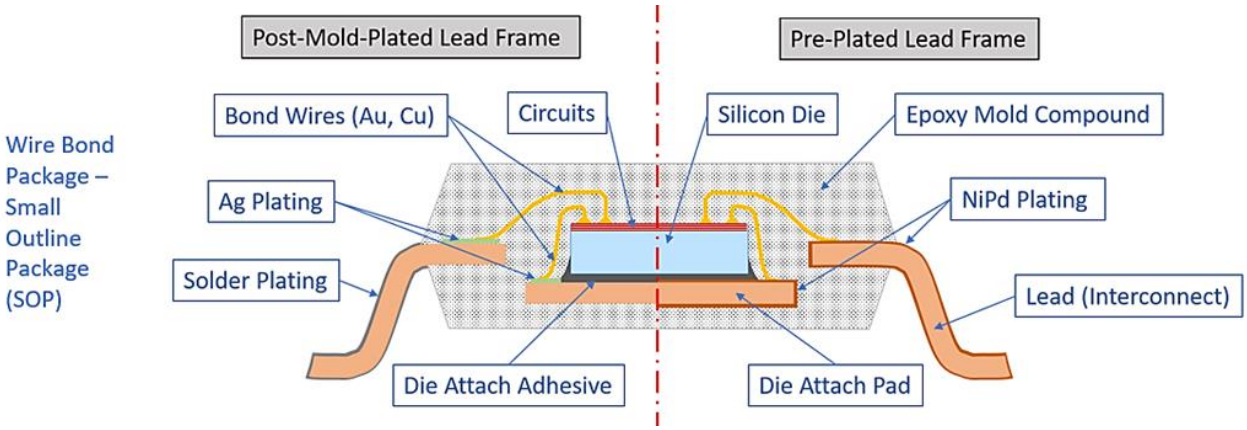


Figure 6: Organic laminate packaging



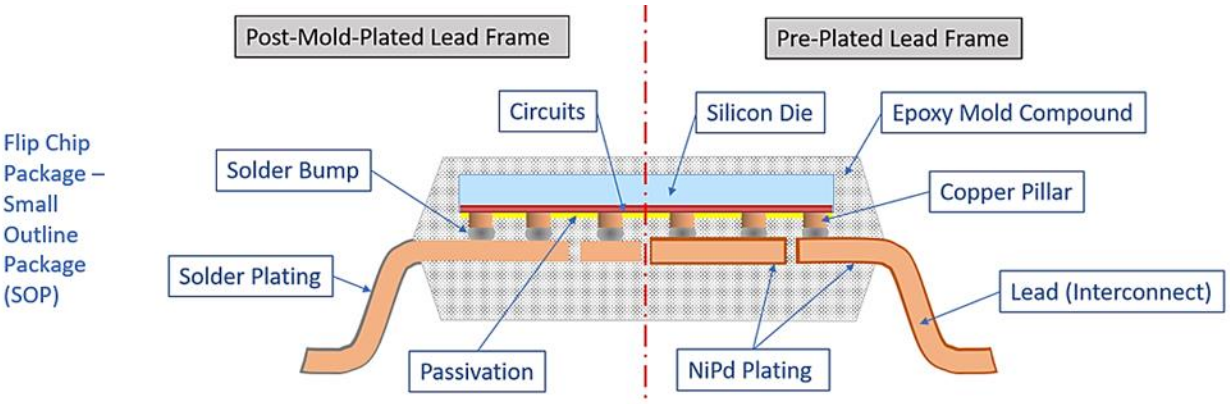
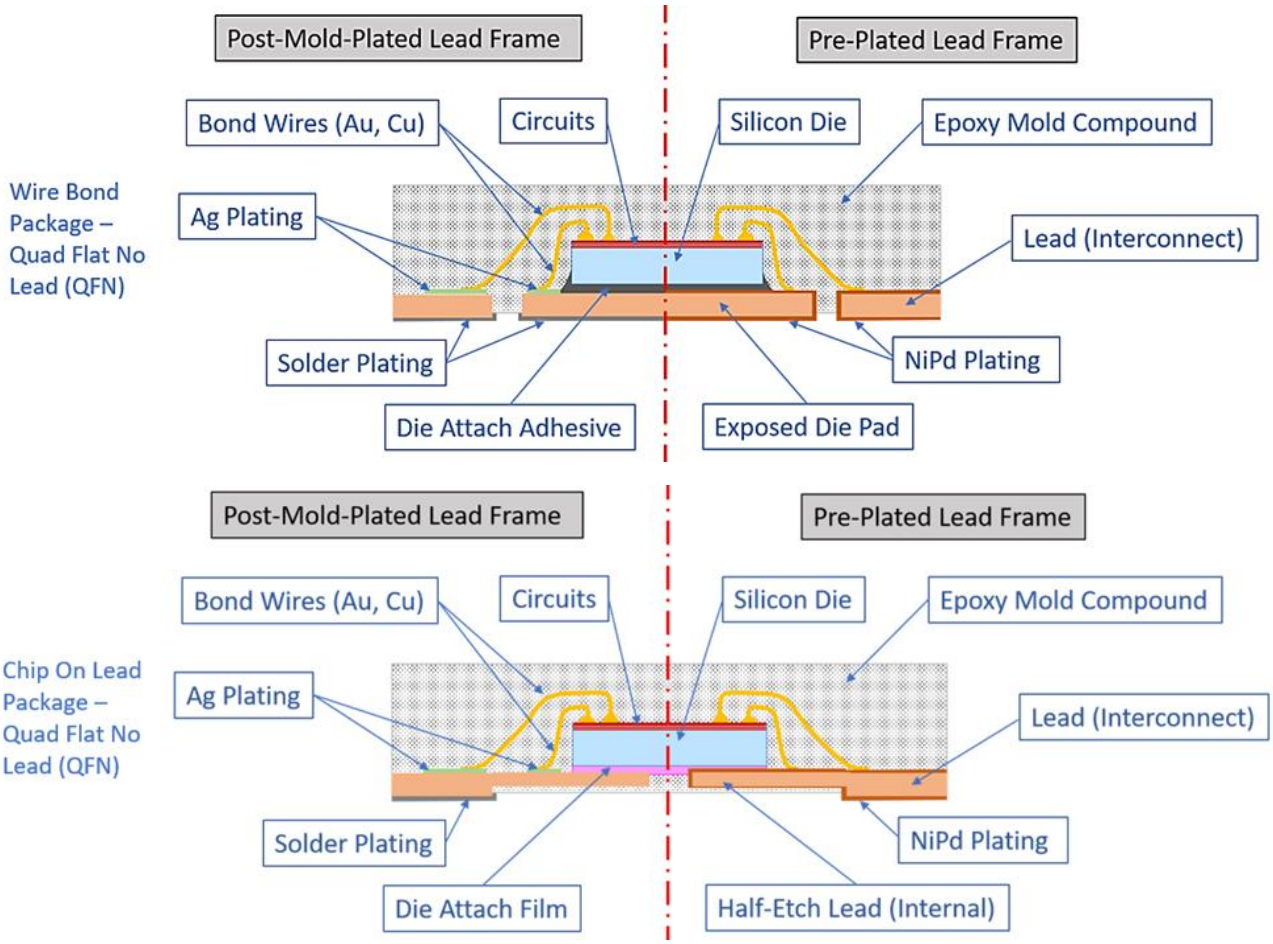


Figure 7: Leadframe packaging (leaded): quad flat pack, small-outline IC



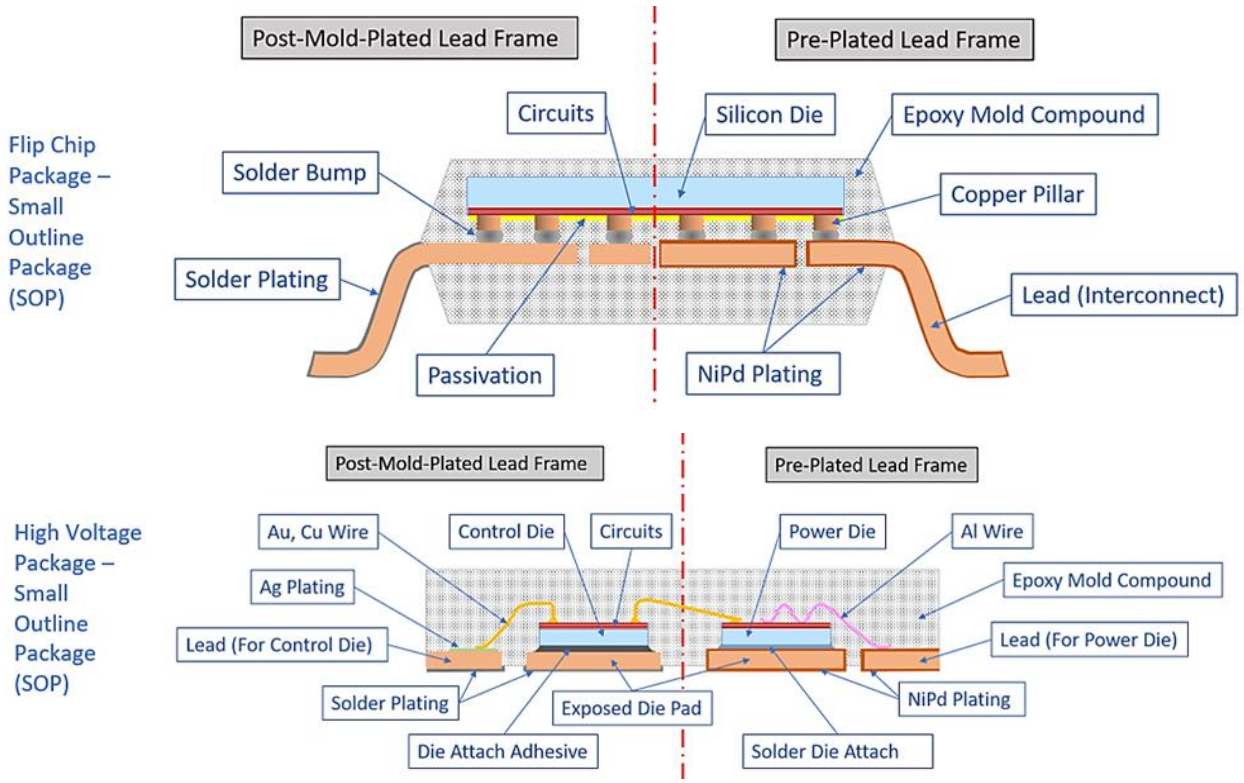


Figure 8: Leadframe packaging (leadless): quad-flat no-lead

Microelectromechanical systems (MEMS) comprise components between 1 and 100 micrometers (µm) in size and usually include a central processor and several components that interact with other devices such as microsensors. MEMS chips (see Figure 9) are often packaged together with an application-specific IC (ASIC) chip stacked together inside the plastic package; combining the sensor and circuitry into one package saves space and cost.

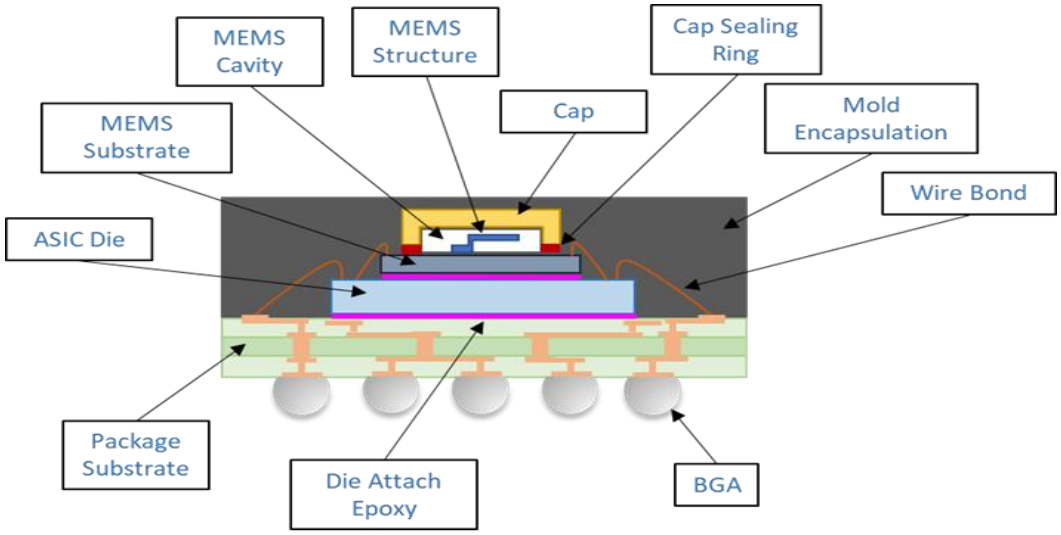


Figure 9: MEMS package diagram

MEMS have widespread applications including as inkjet heads, pressure sensors, microphones, accelerometers, gyroscopes, magnetometers, inertial combs, thermopiles, microbolometers, optical

MEMS, microfluidics, radio-frequency MEMS, oscillators and environmental sensors. MEMS markets include consumer, automotive, industrial, medical, telecommunications, and defense and aerospace (Tasy 1996). The unintentional adhesion of MEMS surfaces is detrimental to performance within the limits of the MEMS actuation and is one of the more pervasive problems with MEMS device fabrication, packaging and handling (Gilleo 2005).

1.3 Use Applications for PFAS-Containing ATPS Manufacturing Materials

PFAS-containing materials are used in ATPS manufacturing environments, support equipment and in manufacturing process materials such as encapsulants, adhesives, coatings, anti-stiction materials and in articles such as substrates and films.

1.3.1 Substrate/PCB

Substrate/PCB is composed of a Core, Buildup/Dielectric and Adhesive Materials. Through patent and literature search, PFAS was identified as present in portions of the substrate.

The mechanical, thermal and electrical functions of substrate materials impose requirements for a high Tg, a low CTE, good thermal and chemical resistance, nonflammability, low moisture absorption, high electrical strength, a low dielectric constant, and dissipation loss (Ho, Leu and Wei 2003).

PFAS-containing substrate materials exhibit low dielectric constants and loss, have low moisture absorptivity, can be used over a wide temperature range, and are nonflammable. PFAS-containing substrate materials are generally not affected by solvents, acids or bases used in substrate manufacturing processes (Morris 2012). Fluorinated materials also have very good dielectric strength (60 MV m^{-1} for PTFE), often making them good insulating materials.

To improve adhesion to unroughened copper (the typical substrate wire component), there is a need to use electron-rich groups/elements such as oxygen- and nitrogen-containing functional groups that can form coordinate bonds with copper. Incorporating these oxygen- and nitrogen-containing functional groups and resins in turn result in increased dielectric loss.

In fluoropolymer-based materials, fluorine atoms can form coordinate bonds with copper to provide the requisite improved adhesion and the low dielectric loss targets (Plenio 2004). The lowest dielectric loss target achieved by a fluoropolymer-based adhesive material with balanced adhesion strengths to copper is ~ 0.0015 at 25 degrees Celsius (°C), with the lowest dielectric constant (Dk) ~ 2.25 at 25°C.

Substrate materials require several properties that can be afforded by PFAS-containing materials, including low electric permittivity (low k or ε_r), low dielectric loss, low water absorption and low coefficient of thermal expansion (CTE), or α. These properties are mentioned in patents from the University of Electronic Science and Technology of China (袁颖林浩东唐斌李恩竹张树人 2017), Jiangxi Tieno Technology Co. Ltd. (余若冰 2017), Intel Corp. (Elsherbini, et al. 2017) and Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC) (Lai, et al. 2013). Buildup (or dielectric) materials within the substrate have the additional property requirements of high adhesion, dimensional stability and reliability. Additional patents detail these buildup material requirements, including Endicott Interconnect Technologies Inc. (Japp, Markovich and Papathomas 2006), Intel Corp. (Starkston, et al. 2016) and TSMC (Wu, et al. 2015). Polytetrafluoroethylene (PTFE), fluorinated ethylene propylene (FEP), perfluoroalkoxy alkane (PFA) and amorphous fluoropolymers are examples of commercially available fluorinated materials.

1.3.1.1 Substrate Core

The core provides strength and rigidity to the substrate. Key characteristics of the core that fluorinated material enhances are the glass transition temperature (Tg), dielectric loss (tan δ), CTE and water absorption.

Fluorinated materials can have a favorable Tg that keeps the material in a rigid glass state during its intended operation and serves as the backbone of the substrate. Typically, the core is composed of a low Tg filler and an epoxide or resin with a similar Tg. As operational ranges increase, the number of materials with an acceptable Tg will decrease.

The Tg of thermoplastic PFAS-containing materials is often below the upper limit of operational temperatures; for example, the Tg of PTFE is 126°C. Above the Tg of a material, its CTE drastically increases, leading to reliability risks. Curing fluoropolymers to create a 3D crosslinked network and incorporating fillers or glass cloth, however, achieves both a high Tg and a low CTE.

Tan δ measures the energy absorbed by the material as an electromagnetic wave passes through that material. The substrate core is subject to significant amounts electromagnetic radiation at a wide frequency range, as information or electromagnetic energy moves into and out of the semiconductor. Many semiconductor products work at very low voltages, making them very sensitive to the adsorption of electromagnetic energy. Current core material has been designed with this constraint in mind. Fluorinated polymers coupled with a nonadsorbing filler offer an attractive pairing to provide both high strength and low electromagnetic absorption.

CTE is the tendency of a material to expand at high temperatures and contract at lower temperatures. Semiconductor products will heat rapidly while operating, as electricity is applied at high frequency. Thus, the materials must maintain their size and shape to prevent failure from electrical shorts, broken connections or varying distances to other features in the product. Fluorinated polymers such as PTFE have a low CTE (Kirby 1956). The fluorinated polymer is typically combined with silica or quartz filler with a particle size <10 μm to create a core at the center of the substrate, stabilizing the product across a wide temperature range.

Water absorption can dramatically affect the dielectric properties of the substrate because of the significantly different dielectric properties of water. An example of the materials used to improve hermitic seals and prevent water absorption is ceramic-filled PTFE, comprising fluoropolymers loaded with fused silica and titanium dioxide (Thompson, Tentzeris and Papapolymerou 2007).

1.3.1.2 Substrate Buildup/Dielectric

The buildup process is the alternating addition of metal and dielectric layers on either side of the core into the final substrate, which is wire bonded to the semiconductor chip. The thickness and number of the dielectric and metal layers depend on the intended performance of the semiconductor; the typical total thickness is >1 millimeter (mm). The dielectric layers must be electrical insulators, have low CTEs matched to the other structures in the package, low water adsorption and ultra-low dielectric loss.

Given the small volume of the substrate, the materials used in the dielectric layer often exhibit all of these properties to ensure intended performance in a relatively small volume. PFAS-containing materials maintain electrical insulation properties across wide temperature and voltage ranges (Sussi and Govinda Raju 1990). Similarly, PFAS-containing materials also have a low CTE (Kirby 1956) and low dielectric loss (Japp, Markovich and Papathomas 2006).

Polyimides are an essential type of buildup dielectrics, owing to their excellent thermal, mechanical and chemical stability as well as their electrical insulation properties. However, because of the high dielectric constant (generally ~3.4 Dk) of these polymers, and the lowered supply of common aromatic polyimide monomers, polyimides are unable to meet the demand for ICs with decreasing sizes and increasing speeds.

Polyimide is a non-PFAS alternative polymer with rigid chain of imide heterocycle, which is composed of binary amine and binary acid/anhydride with large free volume. However, the lowest dielectric loss achieved by polyimide- or nitrogen-oxygen-based adhesives with meeting adhesion targets to copper is in the range of ~ 0.0025 to 0.003 Dk at 25°C, with the lowest Dk 2.6 to 2.75. This clearly shows the need and required use for a PFAS-based adhesive to meet low loss targets of <0.0025 Dk at 90°C and <2.5 Dk at 90°C.

Since the first report of fluorinated polyimides in the 1960s, the incorporation of fluorine atoms by substituting hydrogen and introducing CF_3 substituents has been an effective approach to lower dielectric constants (~2.3 Dk) and to decrease moisture absorption relative to polyimides (Y. Li, et al. 2022). Applying the same strategy to other substrate materials to effectively decrease their dielectric constants has helped meet the urgent demand for smaller and faster semiconductor devices.

In high-speed input/output applications, there is an increased need for dielectric buildup materials to possess low dielectric constants and low dielectric loss. These dielectric materials with ultra-low electrical properties are used in layers, with routing in a substrate package, to meet insertion loss targets. With low electrical targets such as Dk < 2.5 and dielectric loss (Df) < 0.002 at 90°C, there is a need to move from conventional resin systems to ultra-low loss resin systems that are PFAS-based. Most common resin systems used in current low-loss buildup materials are epoxy-based resins and their derivatives. With these resin systems, the lowest dielectric loss possible is in the range of 0.0036 to 0.004 Df at 25°C. For next-generation low-loss targets that incorporate low-loss resins other than PFAS-containing materials, the lowest dielectric loss possible will fall in the range of <0.0021 to 0.003 Df at 25°C. It has been shown in literature that when incorporating fluoropolymer-based resins, the lowest dielectric loss possible is around 0.0014 Df at 25°C. These properties are summarized in Table 1.

Table 1: Comparison of properties for PFAS-containing and non-PFAS containing substrate materials (Li, Sun and Fang 2021) 3.0 Discussion of Potential Alternatives

Property	**Adhesive material with PFAS-containing materials**	**Adhesive material with non-PFAS-containing materials**	**Buildup material with PFAS-containing materials**	**Buildup material with non PFAS-containing materials**
Low dielectric constant (Dk at 25°C)	2.25	2.6-2.75	2.0-2.5	2.6-2.9
Low dielectric loss (Df at 25°C)	0.0015	0.0025-0.003	<0.0014-0.0020	<0.0021-0.003
High adhesion to low-roughness copper pre-HAST conditions in kilograms force per centimeter (Kgf/cm)	0.9	1.3-1.4	–	–

High adhesion to low-roughness copper post-HAST (Kgf/cm)	0.5	0.4-0.7	–	–

Silicone can have low molecular weight siloxanes that could induce contamination throughout the package if used in applications such as mold chase release or other applications to reduce adhesion. Further information is provided in the Mold Compounds, Release Layers and Films section.

As for popular low-loss polymers and their respective properties, the orientation polarization of the intrinsic dipole moments, combined with the dipole polarization of polar functional groups, decisively causes a large increase in dielectric loss. Optimizing the dielectric properties (especially low dielectric loss) requires that polymer chains contain nonpolar functional groups. The position of the polar functional group is also very important: If the polar group is on the side chain of the polymer – especially the flexible polar group, which has strong mobility – it will have a greater impact on the dielectric properties.

PTFE is a nonpolar linear polymer with a highly symmetrical structure comprising two elements: carbon and fluorine. Given the lack of active polar groups, high crystallinity, the high electronegativity of the fluorine atom and the high dissociation energy of C-F bond, this polymer has lower surface energy and higher surface hydrophobicity, making it significantly unaffected by frequency, temperature and humidity.

Olefin polymers are carbon-chain polymers composed only of carbon and hydrogen and lack any polar groups endowing dielectric materials with excellent dielectric properties. Given the small electronic polarizability of C-C and C-H, olefin polymers exhibit low dielectric constant and ultra-low dielectric loss over wide frequency and temperature ranges.

Table 2 shows the dielectric constant and dielectric loss properties of other dielectric polymers. The second column (ε') is the dielectric constant and the third column (tan δ) is the dielectric loss. As can be seen in the table, PTFE has the lowest and most favorable dielectric constant (Wang, et al. 2021).

Table 2: Dielectric properties of select polymers

Polymer	ε'	Tanδ
Polytetrafluoroethylene	2.1	1×10^{-4}
Polypropylene (isotactic)	2.2	1×10^{-4}
Cycloolefin polymer	2.3	2×10^{-4}
Polybutadiene	2.5–2.8	5×10^{-3}
Poly(methyl methacrylate)	2.6	8×10^{-3}
Polyphenylene Oxide (PPE)	3.5	2×10^{-3}
Thermosetting cyanate resin	3.45–3.55	4×10^{-3}–5×10^{-3}
bismaleimide-triazine resin	4.1–4.3	4×10^{-3}–8×10^{-3}

When reviewing potential dielectric material alternatives in the market, there are some that can provide low dielectric constant and low dielectric loss characteristics. None of the alternatives have a lower

dielectric constant and dielectric loss than PTFE, however. Currently, only fluorine-based PTFE can achieve the low-enough values needed to meet next-generation processing and communications.

1.3.1.3 Substrate Adhesive Materials

Adhesive films serve as an intermediate layer to improve the adhesion of dielectric buildup material to ultra-low roughness or unroughened copper. Since adhesive films are used with low-loss-buildup materials, they should possess low dielectric constants and dielectric loss properties to meet the overall insertion loss budget for the product.

There are several versions of fluoropolymer-based organic adhesive materials under development that have shown the lowest dielectric constants and loss properties not seen with other non-PFAS-based adhesive materials. These adhesive materials must possess good adhesion to ultra-low roughness or unroughened copper under extreme environments to minimize any delamination risks in that interface. It has been difficult to balance both low-loss properties and adhesion properties to unroughened copper within the same material with other alternatives.

1.3.2 Die Attach Adhesive

The die attach process bonds the semiconductor die to the substrate for additional processing, and helps transfer heat away from the semiconductor die. Semiconductors designed for power management, computation and dynamic random access memory generate significant heat during operation, requiring the die attach adhesive to have a high heat-transfer coefficient, a low CTE and resistance to thermal fatigue.

Adhesives used for die attach are key direct materials used in the semiconductor assembly process. These adhesives attach semiconductor chips or silicon die to packaging substrates and leadframes. In addition to forming the attachment, they can help mitigate stress and control warping during system operation. In some applications, the die attach adhesives form a path to conduct heat from the chip to a heat sink.

Fluorinated polymers can have both a low CTE and resistance to thermal fatigue, making them an ideal constituent in die attach adhesives. Current die attach adhesives emerged in response to the Restriction of Hazardous Substance Directive (RoHS), adopted in 2003 by the European Union. Before implementing RoHS, die attach adhesives were predominantly leaded solders. To conform to RoHS and limit exemptions, chemists developed die attach adhesives using fluorinated polymers with silver or other metals to create materials with a high heat-transfer coefficient, a low CTE and resistance to thermal fatigue.

PFTE is an additive in some die attach adhesives to add specificity in polymerization by limiting the area of the flow of the adhesive or bleed control. These PFTE “anti-bleed agents” (or anti-epoxy bleed out [EBO]) control the amount of epoxy bleed beyond the peripherals of the die mounted to the leadframe/substrate. This is essential in order to prevent the epoxy from spreading to adjacent critical areas such as wire-bond pads, which will lead to product failures such as wire non-stick on pad (NSOP) or spread on the die top, resulting in a lack of mold compound adhesion and subsequent void and delamination on the package. The PFTE also promotes flatness of the die and a uniform adhesive thickness (Zhang, Castro and Lin 2017). Fluorine-containing chemicals are well known for low surface energy. For example, poly(hexafluoropropylene) has a critical surface tension of 16.9 dyne per centimeter (dyn/cm), while polydimethylsiloxane has a critical surface tension of 20.1 dyn/cm (AccuDyneTest 2023). Die attach paste, encapsulant and underfill material sometimes employ PFAS surfactants in quantities less than 0.1% total weight in order to meet performance requirements for ATPS applications.

While supporting literature describing these uses of anti-bleed agents as necessary is not available, industry practice has proven these to be critical in some cases to resolve device failure issues associated with adhesive bleed during its application. Further research will be required to determine if non-PFAS alternatives can be effective in these applications.

1.3.3 Encapsulants

Encapsulants provide environmental and mechanical isolation of semiconductors and wire bonds in addition to heat conductivity to ensure optimum semiconductor performance. Encapsulants must have a low CTE across a wide temperature range without a Tg in the operational range of the semiconductor package. The Tg is the temperature at which there are significant changes in the material's thermal, mechanical and thermomechanical properties.

Fluorinated polymers exhibit low CTE without a Tg, while being an excellent electrical insulator. These properties make PFAS-containing materials an attractive constituent for encapsulants. Additionally, PFAS-containing materials can be hydrophobic, which is an ideal property in encapsulants because a common failure mechanism for encapsulants is void creation caused when water absorbed by the encapsulant expands during heating caused by operation of the semiconductor (Thompson, Tentzeris and Papapolymerou 2007). Hydrophobic encapsulant constituents minimize the amount of water absorbed, reducing the opportunity for failure.

Some cured adhesives need to be chemically resistant. Dow Silicones Corp. details the use of fluorosilicone elastomers in order to improve chemical resistance in an electronics adhesive (Ahn and Rolley 2003). They also discuss the need for flexibility and bulk thermal properties that are possible through the use of fluorinated acrylates. A fluorocarbon-based film may also act as a gas barrier for water or steam, as detailed in 3M's patent (マコーミック, フレッド 2009).

1.3.4 Release Layer

Fluorinated polymers are promising candidates for "anti-adhesion" or release layers for temporary bonding debonding (TBDB). TBDB requires an adhesive that can maintain an appropriate bond strength between the device wafer and the carrier through subsequent processing such as wafer thinning. After the required processing, the device wafer must be released from the carrier. One common release method is mechanical release, which is initiated by the insertion of a razor blade between the two wafers, with full separation achieved through subsequent lift off the wafer. Another method of release is to use a low-surface-energy material as the release layer. Fluorocarbon polymers are one such class of polymer that offer attractive properties (Schelcher, Brault and Bosseboeuf 2011) and (AccuDyneTest 2023).

It is also possible to use fluorinated polymers in laser release layers, but here the function is more for UV light sensitivity than mechanical debonding. Because these layers are sometimes iterations on front-end or lithography-type materials, the UV sensitivity can be tuned using PFAS-containing materials. With their known ability to aid in photoacid generation efficiency, UV release layers can also benefit from PFAS-containing materials to remove adhesive from wafers or other pieces cleanly.

1.3.5 Adhesive Tapes

Using fluorine-based materials as a release agent can prevent adhesion between the adhesive and the film (아사이 2010). This same patent discusses the use of PFAS-containing materials as a pressure-sensitive adhesive.

As a generic adhesive, PFAS-containing materials can help prevent sticking of thermal or UV-curable materials to an applicator during processing. Another use of PFAS-containing materials could be to inhibit dripping during processing, as described by Teijin Ltd. (Inazawa and Ishida 2012).

1.3.6 Flux

PFAS-containing surfactants are typically more heat-resistant, with wetting properties that control spread. By using a PFAS-containing material in an application that applies a flux to metal bumps between the die and the substrate before reflow, the heat resistance (the thermal stability of the flux) preserves the activity of the flux during the high temperature encountered during reflow of the assembly. PFAS addition also aids in controlling degradation that may cause residue within the solder joints or residue that remains on the package or die, causing voids during underfill. These voids, in the solder joint or in the underfill, affect package reliability and yield.

PFAS-containing chemicals can help control flux spread during high-temperature exposure, so that the flux can remain in the solder joint area during soldering and improve the solder joint quality and yield. An Arakawa Chemical Industries Ltd. patent discusses this reduction of voids in the solder (Fumio Ishiga 2005). PFAS-containing materials can be used in fluxes as surfactants, as discussed by patents from Freescale Semiconductor Inc (웨츠리안 2002) and IBM (Richard Martin 1970).

1.3.7 Cleaning Chemistry/Process Steps

In the substrate process flow, there is a need to remove dielectric material, using a dry plasma process to clean debris of an existing pattern (via) or to form some pattern structure within the dielectric material layer. The most popular dielectric material in substrate is a filled system, with silicon dioxide as an inorganic filler in organic polymer resin. The etching process includes the removal of silicon dioxide. The common plasma gases for silicon dioxide etching are tetrafluoromethane (CF_4), trifluoromethane (CHF_3), hexafluoroethane (C_2F_6) and hexafluoropropene (C_3F_6). The dominant reactive species are CFx, which produces the etched products silicon tetrafluoride (SiF_4), carbon monoxide (CO) and carbon dioxide (CO_2).

Plasma processing for etching typically uses fluorine-based etching gases because fluorine atoms are the most reactive among all halogens on silicon. Currently, there is no alternative gas to be used for dry plasma etching to remove silicon dioxide.

1.3.8 Die Overcoat/Adhesive

Packaging applications need hermetic and chemical resistance adhesive coatings. PFAS-containing chemicals impart chemical resistance and hydrophobicity in chemical- and moisture-sensitive applications.

Adhesive materials required for use in semiconductor packaging must have the ability to simultaneously meet ultra-low dielectric constant property targets as well as reliability requirements such as adhesion to ultra-low roughness and unroughened copper under high-humidity, high-temperature conditions. When using highly accelerated stress testing (HAST) to predict field performance, low adhesion to copper will cause early HAST failures.

1.3.9 Underfills

Underfills are typically polymer materials that bind the package to the PCB and reduce stress on the solder joints. They increase the semiconductor durability and the life span of the assembled package compared to an assembled package without an underfill.

Because the underfill sits between the package and the PCB, it must have high mechanical strength and low CTE. Underfill will contain approximately 50% silica materials, with the remainder polymeric materials with high viscosity and low volatility. A high viscosity ensures homogenous distribution of silica materials during curing, while low volatility minimizes void formation that can cause failures

during temperature cycling. Toray Industries (金森大典 2014) described using a fluoropropyl group to form a semisolid film on the chip surface to improve mechanical strength and reliability.

Using a semisolid polymer structure of fluorinated rubbers such as vinylidene fluoride-propylene hexafluoride copolymer and tetrafluoroethylene-propylene copolymer provides stress relief for the solder joints, as described by Namics Corp. (파웰 츄바로우 2011).

PFAS-containing surfactants aid in the manufacture of epoxy materials to prevent air bubbles. They are more inert in high-temperature conditions during underfill curing, which provides greater compatibility of the additive with the resin system and helps control resin bleedout.

1.3.10 Mold Compounds, Release Layers and Films

Mold compounds are used as a protective outer layer covering most or all of the semiconductor package substances (see figure 6-9). The mold compound is injected into a mold chase that includes the semiconductor and package elements. PFAS-containing materials are thermally stable and provide a cleaner release from the mold chase or film. The materials - PTFE or ethylene tetrafluoroethylene (ETFE)- can be in either the release film or the mold itself.

A release sheet for power module molding which contains PFTE is used to prevent materials from adhering to the mold itself. It is applied to the mold between each molding cycle and comes off on the molded product. A buffer sheet for power module thermocompression bonding (sintering) also contains PFTE. PTFE is essential for release sheets and there are currently no known alternatives.

The functionalities required and provided using PFTE in these films are:

- Heat resistance, flexibility, and separation or release at a temperature range of 175℃ to 300℃
- Sheet strength integrity to avoiding breakage
- Separation or release to peel off the sheet from the sealing resin, chip, or mold.

A mold release spray, similar in functionality to nonstick cooking spray, also contains and requires PFAS materials. Alternative materials such as silicone can result in contamination in other parts of the process, tools or package, and delamination of downstream material additions.

Another functionality of PFAS-containing materials is used as a catalyzer for a cured epoxy. Nippon Shokubai Co. Ltd. discusses the use of sulfonic acids or boron trifluoride to act as ion exchange resins (杉冈卓央 2005). This same patent discusses the use of fluorocompounds in small percentages to thin the epoxy but maintain the overall epoxy characteristics.

PFAS-containing materials are known to be thermally stable and provide the required flame retardancy. Teijin Chemicals Ltd. discusses the use of PTFE to improve flame retardancy (Hisanaga Shimizu 1989) and (Yasunori Inazawa 2012).

1.3.11 Thermal Interface Materials

In order to prevent dual-layer thermal interfaces from ripping, tearing or otherwise losing or disrupting their dielectric or thermal properties during assembly, the material-comprising layer must be tear-resistant and have a high tensile strength. The incorporation of highly thermally conductive fillers such as carbon nanotubes, metals and ceramics into different resin systems may require a compatibility that only FEP can impart – as explained by Asiapack Holding SA (Thomasset 2007).

Fluorocarbon resins, fluororesins or fluorinated polyallyl ether resins help achieve high thermal conductivity and can also help hold the components during processing due to high viscosity and elasticity. These properties are described by Tesla Motor Co. (Hermann 2010) and Cabot Corp (バーニー，アンドレア 2008).

1.3.12 Photo-Acid Generators

Photoresists are used in C4 and many advanced packaging processes and rely upon photo-acid generators to initiate the polymerization reaction. Several photo-curable or patternable materials use photo-acid generators, which contain perfluorinated compounds, as initiators (Ober, Kafer and Jingyuan 2022).

1.3.13 Anti-Stiction and Wear Resistance Agents in Certain MEMS Devices

Stiction, or static friction, is the sticking or locking together of relatively smooth surfaces that come together (Tasy 1996). The unintentional adhesion of MEMS surfaces is irreversible within the limits of MEMS actuation and is one of the more pervasive problems with MEMS device fabrication, packaging and handling (Gilleo 2005).

Wear is a phenomenon associated with rubbing or impacting surfaces that can be a concern in MEMS devices with sliding elements. There are four main causes of wear: adhesion, abrasion, corrosion and surface fatigue. Applying protective interfaces to MEMS structures such as deposition of a PFAS coating reduces wear failures (Huang, et al. 2012).

PFAS-containing materials are used in the packaging of MEMS devices for surface energy modification for anti-stiction purposes. Traces of the PFAS-containing material may remain inside the package when it is formed; however, this would be less than 0.1% by weight (w/w) in each MEMS device. As a consequence of trace amounts of residue, the amount of PFAS-containing materials in MEMS devices across all semiconductors is estimated to be less than 1 kg per year, as described in a pending patent from TSMC. (Jui-Chun Weng 2018).

1.3.14 Thermal-Acid Generators

Photoresists are used in many advanced packaging processes and rely upon thermal-acid generators to initiate the polymerization reaction. Many solution-processable materials require thermal-acid generators, which are often quaternary ammonium triflate salts for crosslinking or curing.

1.3.15 Surfactants

Surfactants can play many roles. One is as an additive in solution-processable materials to assist in coat quality during spin-on processes. PFAS-containing surfactants can also aid in the manufacture of epoxy or adhesive materials to prevent air bubbles.

1.3.16 Die Passivation

PFAS-containing materials are used as part of the controlled collapse of chip connection (C4) bumping process that connects the chip to the interposer. A photoimageable dielectric is used to both help pattern the bumps and to remain on the die and protect the interlayer dielectric (underlying electronics within a die). This photoimageable dielectric requires similar properties to existing photolithography materials that contain PFAS-containing materials to process the fine features needed. This protection layer also needs thermal and chemical stability that PFAS-containing materials impart. Common die passivation layers in the industry such as polyimide, polybenzoxazole and other epoxy-based passivation all contain PFAS-containing materials, and there are no known alternatives.

Photoresists are used in assembly packaging for wafer-level assembly, substrate manufacturing and C4 bumping. For more information about photolithography, see "Review of essential use of fluorochemicals in lithographic patterning and semiconductor processing." (Ober 2022).

1.4 Critical Performance Requirements Met by PFAS-Containing ATPS Manufacturing Materials

This series of tables lists the critical performance requirements:

- Appendix A1 is for adhesive-type materials (including underfill and mold).
- Appendix A2 is for additional assembly materials (such as fluxes and thermal interface materials). Appendix A3 is for substrate materials.
- Appendix A4 is a summary table of additional properties.
- Appendix B provides some definitions of the materials in Appendix A4.

A key performance metric that enables such high-speed communication is the insertion loss metric. Insertion loss is a very important performance metric for high-speed communication. The lower dielectric constant and dissipation loss of PFAS-containing materials enable low insertion loss (high-frequency signal transmission loss). The lower the dielectric constant and dissipation loss, the lower the insertion loss in a package. With exponential growth of data generation and transmission, the need to handle high-bandwidth communication within and between microprocessor packages and between microprocessors and memory components necessitates high-frequency and high-speed communication. Areas of artificial intelligence and data analytics benefit greatly from high-speed electronics and microprocessors. Operating these devices at lower speeds can have adverse effects. Additionally, data center power use and increased power consumption of computational devices is a growing area of concern with respect to energy supply and consumption. The lower insertion loss enabled by PFAS-containing materials can significantly reduce energy consumption rates.

On the other hand, PFAS-based resin systems have the lowest dielectric loss properties compared to other alternatives that can achieve ultra-low electrical property targets needed for next-generation buildup materials. Table 3 provides information on applicable properties for PFAS-containing adhesive and buildup materials.

Table 3: Required properties for adhesive and buildup materials

Property	Adhesive material with PFAS-containing materials	Buildup material with PFAS-containing materials
Low dielectric constant	X	X
Low dielectric loss	X	X
High adhesion to low-roughness copper (pre-HAST conditions)	X	
High adhesion to low-roughness copper (post HAST)	X	

Current high-speed PCBs use PFAS-containing materials such as PTFE or other similar fluorinated-containing organic polymers to enable high-speed signaling between the components of a module or an assembly. This is mainly because PCB conductor lengths are long, and longer travel distances exacerbate signal loss. Fluorinated components offer best-in-class electrical properties for dielectric constant and insertion loss. No other manufacturable material currently exists that enables faster signal processing as frequencies increase.

Signal-processing and frequency requirements will not only mandate the use of fluorinated materials on PCBs and PCB materials (such as glass-reinforced components); they will also move the requirements upstream into packaging materials such as buildup and adhesive. Specifically, as the signalling frequency increases the conductor length becomes even more critical; higher losses require lower insertion loss materials. It may also be the case that in certain packaging applications that need high-speed signaling on the core or on package architectures such as package-on-package or interposers (where the material used is a glass-reinforced epoxy matrix), PFAS-containing materials are one possible path to mitigate the risk of signal loss.

1.5 Role of the Fluorine Atom and C-F Bond

The compact size of the fluorine atom and its strong electron-withdrawing characteristics make many unique and essential properties of PFAS ATPS materials used in the semiconductor industry possible. (Kirsch 2004, 1-23)

The fluorine atom imparts a number of unique and beneficial properties to PFAS-containing materials. No other nonfluorinated compound can claim a similar set of properties together in the same material. The first effect of F is to strengthen the C-F bonds and to impart excellent thermal, oxidative and chemical stability. The second effect is to shield the carbon skeleton of the molecule, contributing to the exceptional chemical stability and nonflammability. Third, the low polarizability of the C-F bond and the bulkiness of the CF_3 group explain the extremely low dielectric constant of PFAS-containing substrate materials. The hydrophobicity of PFAS (attributed to the low polarizability of fluorine) also minimizes moisture absorption and enhances the stability of dielectric properties of the material in humid environments. For more information, see Background on Semiconductor Manufacturing and PFAS.

2.0 Potential Areas of Research and Development

Semiconductor packaging applications use PFAS-containing materials to provide a number of essential functions in a range of packaging structural elements, including package substrates, redistribution layers, fluxes, adhesives, underfills, electronic mold compounds, dielectrics and thermal interface materials. Given the public health concerns related to the use of PFAS compounds, there is need for research on the development, maturation and characterization of materials and their performance in a number of use cases.

Specific technology gaps related to non-PFAS-containing materials, for which research is suggested:

- The definition and formulation synthesis of non-PFAS-containing materials with performance comparable to PFAS versions.
- The material performance of new non-PFAS-containing materials relative to PFAS-containing versions in cases where non-PFAS-containing materials have been invented, tested and qualified (with years of historical data and field performance).
- Non-PFAS-containing material compatibility and performance, including adhesion to other materials such as solder masks and smooth low-roughness copper.
- Performance and reliability predictive models in a number of use-case scenarios relevant to high-volume applications.
- Non-PFAS-containing packaging performance at sustained high temperatures, low temperatures, wide thermal excursions and large thermomechanical loads.
- While unexpected to cause any risk to human health and the environment, an evaluation of whether PFAS included in de minimis amounts in finished semiconductors poses any impact during or at the end of the product’s useful life.

3.0 Health and Safety Concerns

In all semiconductor manufacturing, regardless of the level of sophistication of the factory, equipment systems operate with intrinsic controls that minimize or control chemical liquid or vapor exposure potential during normal equipment operations. The equipment must be maintained frequently, which requires placing the operating parts of the equipment on standby (nonoperating mode) and opening protective enclosures.

During these maintenance activities, workers use protective equipment to reduce the potential for employee exposure. In all cases, a high degree of engineering controls minimizes employee exposure, including exhaust, interlocks and monitoring. Where engineering controls are not available, administrative controls minimize the potential for exposure. For additional detail, see the Background on Semiconductor Manufacturing and PFAS.

4.0 Environmental Releases and Controls

There has not been a large-scale investigation in the waste streams across the ATPS supply chain for the broad definition of PFAS used in this paper. Because the materials have not been regulated, there has not been the same traceability for multiple PFAS compounds as there has been for other compounds regulated or traced in the ATPS space. There is not a database of leaching data for most PFAS-containing materials; therefore, leaching studies are not included here. This is an area in ATPS needing further investigation and research. For additional detail, see the Background on Semiconductor Manufacturing and PFAS.

4.1 Potential Releases During Use

For other product compliance purposes, the industry has been collecting bill of material information. Most PFAS we've identified through the consortium work are not listed on the bill of material received by device manufacturers; however, patent and literature searches indicate they may be present. From the information we have received through bill of material and surveys, concentrations of PFAS containing materials are low, and any releases are anticipated to be in the de minimis range. In the case of end products, there should be no release of PFAS-containing materials to consumers during normal use.

4.2 Potential Releases During End of Life

PFAS-containing materials could remain in the final product during its life but, because the uses are sealed inside the package and those packages are inside an electronic device, they are unlikely to cause direct exposure to the consumer. Because of the de minimis quantities that may be contained in the package, it is unknown if end of life controls are necessary during the reclamation of electronic products.

5.0 Conclusions

ATPS has unique thermal, chemical and electrical requirements for which use of PFAS materials are essential. There are a wide variety of semiconductor assembly processes and many different types of packages. This, coupled with a complex manufacturing ecosystem make investigation into PFAS use and replacement challenging to review.

Based on patent searches and discussions with experts, substrates/PCBs, encapsulants, release layers, adhesive tapes, fluxes, overcoats, cleaning chemistry, mold compounds, release layers/films, thermal interface materials, photo and thermal acid generators, surfactants and some photoimagable dielectric used in die passivation require the use of PFAS to meet the needed performance requirements. Some manufacturing flows currently use PFAS-containing adhesive anti-bleed agents without proven replacements. Similarly, some advanced MEMS applications require PFAS-containing materials to meet demanding conditions where their use has been proven to be irreplaceable. There are currently no known

alternatives to PTFE used in the applications of release sheet for power module molding and buffer sheets used for power module thermocompression bonding (sintering).

Research is needed on non-PFAS alternatives to identify their viability to achieve performance, as is reliability data. This white paper identified some of the technical gaps requiring further research. There is also a need to build knowledge within the ATPS supply chain and perform further investigation into alternatives, life-cycle analysis and treatment.

6.0 References

AccuDyneTest. 2023. *Critical Surface Tension and Contact Angle with Water for Various Polymers.* https://www.accudynetest.com/polytable_03.html?sortby=cst%20ASC.

Ahn, Dongchan, and Patricia Ann Rolley. 2003. EP Patent 1660572B1.

Elsherbini, Adel A., Henning Braunisch, Aleksandar Aleksov, Shawna M. Liff, Johanna M. Swan, Patrick Morrow, Kimin Jun, Brennen Mueller, and Paul B. Fischer. 2017. US Patent 11348897B2.

Fumio Ishiga, Yasuo Chiba, Kajita Kazunari. 2005. China Patent CN101090797B.

Gilleo, Ken. 2005. *MEMS/MOEMS Packaging: Concepts, Designs, Material, and Processes.* N.Y.: McGraw-Hill.

Hermann, Weston Arthur. 2010. United States Patent US8263250B2.

Hisanaga Shimizu, Koji Ishihata, Kazuo Kitamura. 1989. Japan Patent JPH02199162A.

Ho, Paul S., Jihperng Jim Leu, and William Wei. 2003. *Low Dielectric Constant Materials for IC Applications.* Berlin, Heidelberg: Springer.

Huang, Yunhan, Arvind Sai Sarathi Vasan, Ravi Doraiswami, Michael Osterman, and Michael Pecht. 2012. "MEMS Reliability Review." *IEEE Transactions on Device and Materials Reliability* 482-493.

Inazawa, Yasunori, and Masashi Ishida. 2012. US Patent 9732219B2.

Japp, Robert M., Voya R. Markovich, and Kostas I. Papathomas. 2006. US Patent S7429789B2.

Japp, Robert M., Voya R. Markovich, and Kostas I. Papathomas. 2006. US Patent 7429789B2.

Jui-Chun Weng, Lavanya SANAGAVARAPU, Ching-Hsiang Hu, Wei-Ding Wu, Shyh-Wei Cheng, Ji-Hong CHIANG, Hsin-Yu Chen, Hsi-Cheng Hsu. 2018. United States Patent US20220242724A1.

Kirby, Richard K. 1956. "Thermal Expansion of Polytetrafluoroethylene (Teflon) From-190 to +300 C." *Journal of the National Bureau of Standards.*

Kirsch, Peer. 2004. *Modern Fluoroorganic Chemistry: Synthesis, Reactivity, Applications.* Weinheim: Wiley-VCH Verlag GmbH & Co. KGaA.

Lai, Jui Hsieh, Ying-hao Kuo, Hai-Ching Chen, and Tien-I Bao. 2013. US Patent 10261248B2.

Li, Minghui, Jing Sun, and Qiang Fang. 2021. "A fluoropolymer with a low dielectric constant at a high frequency derived from bio-based anethole." *Polymer Chemistry* 12, 4501-4507.

Li, Yahui, Gaohui Sun, Yu Zhou, Guangmin Liu, Jun Wang, and Shihui Han. 2022. "Progress in low dielectric polyimide film–A review." *Progress in Organic Coatings* 172.

Lo, H. Louis, and Bok Eng Cheah. 2015. "Study of conductor surface roughness impact on package insertion loss." *IEEE 17th Electronics Packaging and Technology Conference.*

Martin, S. J., , J. P Godschalx, M.E. Mills, E.O. Shaffer II, and P.H. Townsend. 2000. "Development of a Low-Dielectric-Constant Polymer for the Fabrication of Integrated Circuit Interconnect." *Advanced Materials* 1769-1778.

Morris, James E. 2012. *Electronics Packaging Forum.* New York, NY: Springer.

Ober, Christopher, Florian Kafer, and Deng Jingyuan. 2022. "Review of essential use of fluorochemicals in lithographic patterning and semiconductor processing." *Journal of Micro/Nanopatterning, Materials, Metrology.*

Plenio, Herbert. 2004. "The Coordination Chemistry of Fluorine in Fluorocarbons." *Specila Issue: Flourine in the Life Sciences* 650-655.

Richard Martin, et al. 1970. Germany Patent DE2137329A1.

Schelcher, G., S. Brault, and A. Bosseboeuf. 2011. "MEMS Process by Film transfer Using a Fluorocarbon Anti-Adhesive Layer." *Journal of the Electrochemical Society* 158 () pp H545-550.

Starkston, Robert, Robert L. Sankman, Scott M. MOKLER, Richard Christopher Stamey, and Amruthavalli Pallavi Alur. 2016. US Patent 11114353B2.

Sussi, M. A., and G. R. Govinda Raju. 1990. "Electrical conduction current in polytetrafluoroethylene." *Annual Conference on Electrical Insulation and Dielectric Phenomena.* 196-201.

Tasy, N., Sonnenberg, T., Jansen, H., Legtenberg, R., Elwenspoek, M. 1996. "Stiction in Surface Micromachining." *Journal of Micromechanics and and Microengineering* 6, 385.

Thomasset, Jacques. 2007. United States Patent US8623250B2.

Thompson, Dane, Manos Tentzeris, and John Papapolymerou. 2007. "Experimental Analysis of the Water Absorption Effects on RF/mm-Wave Active/Passive Circuits Packaged in Multilayer Organic Substrates." *Advanced Packaging* 551-557.

Wang, Lu, Jing Yang, Wenhua Cheng, Jiajia Zou, and Dan Zhao. 2021. "Progress on Polymer Composites With Low Dielectric Constant and Low Dielectric Loss for High-Frequency Signal Transmission." *Frontiers in Materials.*

Wu, Chih-Wei, Jing-Cheng Lin, Szu-Wei Lu, and Ying-Ching Shih. 2015. US Patent 9704825B2.

Yasunori Inazawa, Masashi Ishida. 2012. United States Patent US9732219B2.

Zhang, Rongwei, Abram Castro, and Yong Lin. 2017. *Solutions for controlling resin bleed out.* 12. https://sst.semiconductor-digest.com/2017/12/solutions-for-controlling-resin-bleed-out/.

バーニー，アンドレア, エイチ．スワループ，スリニバスエイチ．スワループ，スリニバスディー．デイビス，ティモシーディー．デイビス，ティモシーオー．バーニー，アンドレアオー．. 2008. Japan Patent JP5931129B2.

マコーミック，フレッド, 藤田　　淳多門 田寺ビー．. 2009. JP Patent 5270755B2.

아사이, 나오히데 다카모토고지 시가후미테루. 2010. KR Patent 101933339B1.

웨츠리안, 케서리자베쓰안,바자즈라지브,팡트렐리안트. 2002. Korea Patent KR100985004B1.

파웰 츄바로우, 오사무 스즈키, 도시유키 사토, 카즈요시야마다, 가오리 마츠무라, 나오키 오바타. 2011. Korea Patent KR101900534B1.

余若冰. 2017. CN Patent 106604536B.

杉冈卓央, 辻野恭范. 2005. China Patent CN102337005B.

袁颖林浩东唐斌李恩竹张树人. 2017. CN Patent 107474312B.

金森大典, 小田拓郎, 野中敏央. 2014. China Patent CN105745274B.

Appendix A1: Critical Performance Requirements Met by PFAS-Containing Materials in ATPS Materials: Adhesive-Type Materials

Property	UV-Curable adhesive	Release layer	Adhesives (various)	Die overcoat	Mold, molded underfill, mold release layers and films	Underfill and epoxy materials
Adhesion	High shear adhesion Adhesion at room temperature Adhesion to silicon	Anti-adhesion or release: mechanical separation of adhesive			Heat resistance, flexibility, and releasability	Prevent delamination
Chemical and corrosion resistance	Chemically resistant			Chemically resistant		
Cleanliness	Reduce foreign material Low residue transfer	Clean removal Minimal residue			Cleaner release from mold chase or film prevents contamination downstream	
Dielectric constant			Low			
Flame retardancy						Some flame retardancy
Hydrophobicity				Repels or does not absorb water		
Manufacturing considerations						Prevents air bubbles during manufacturing of epoxy or adhesives
Material flow					Ease of flow in mold chase	
Nonstick/low surface energy		Low surface energy				
Oxidative stability			High stability			
Photoactive			Photoactive adhesive			
Repellency: water, oil						Resistant to grease/stains
Solubility			Soluble in organic solvents			

Property	UV-Curable adhesive	Release layer	Adhesives (various)	Die overcoat	Mold, molded underfill, mold release layers and films	Underfill and epoxy materials
Surfactants					Ease of underfill processing	
Thermal stability (low and high temperatures)			High thermal stability		Thermally stable	Inert to high temperatures and more compatible with resin systems
UV resistance/UV transparency	UV curing	UV curing of adhesive				
Wetting/spread						Reduces or prevents resin bleedout

Appendix A2: Critical Performance Requirements Met by PFAS-Containing Materials in ATPS Materials: Additional Assembly Materials

Property	Flux	Thermal interface materials	Die passivation	PCB	MEMS
Chemical and corrosion resistance			Chemically stable through multiple downstream process steps	Chemical resistance	
Cleanliness	Low residue – controls degradation of flux during processing				Low residue build up on mechanical components
Compatibility		Incorporation of various fillers into different resin systems			Inert to structural components and other materials
Dissipation (ratio of capacitive reactance to resistance at a specified frequency)				Low dissipation	
Flame retardancy				Some flame retardancy	

Property	Flux	Thermal interface materials	Die passivation	PCB	MEMS
Frequency				High frequency	
Heat transfer properties		Heat resistance High thermal conductivity		Heat resistance	
Manufacturing					Molecular stability
Material flow		Improved material flow No pump-out			
Nonstick/low surface energy	Preventing (over)spreading	Good wetting			Low surface energy anti-stiction internal surface coating
Repellency: water, oil				Water and oil repellent	
Surfactants	Reduce residue after reflow	Surfactant to align molecules			
Thermal stability (low and high temperatures)	Reduce volatilization at higher temperatures/maintain flux activity at higher temperatures	Heat resistance	Thermally stable through multiple downstream process steps and active life of product	Heat resistance	Resistance to degradation in the presence of high levels of electromagnetic radiation or flux
UV resistance/UV transparency			Photoimageable		
Wear resistance					Prevents component wear throughout normal high movement frequency operation
Wetting/spread	Controls spread				

Appendix A3: Critical Performance Requirements Met by PFAS-Containing Substrate Materials

Item	Condition	Target
Loss tangent (cavity perturbation)	1 GHz (at 90°C)	≤0.002
10 GHz (at 90°C)	≤0.002	
56 GHz (at 90°C)	≤0.002	
90 GHz (at 90°C)	≤0.002	
Dielectric constant (cavity perturbation)	1 GHz (at 90°C)	≤2.0
10 GHz (at 90°C)	≤2.0	
56 GHz (at 90°C)	≤2.0	
90 GHz (at 90°C)	≤2.0	
Surface roughness post-dry desmear across 510-mm × 515-mm panel, (Ra) mean	Nanometer	<50
Via size formed: CO_2 laser drilling process	Micrometer	<60 µm
Via size formed: UV laser drilling process	Micrometer	<30 µm
CTE x-y (ppm/°C)	T = 25°C-150°C	alpx, alpy <20
	T = 150°C-240°C	alpx, alpy <40
Tg (°C)	Dynamic mechanical analysis	150-200
	Thermomechanical analysis	150-200
Young's modulus (GPa)	25°C	<13
Fracture toughness (K_{IC}) (MPa.m1/2)	25°C	>1.0
Elongation at break (%)	25°C	>1
Minimum melt viscosity during processing window (poise)		<2,000
Water absorption (%)	100°C, 1 hour	<0.5
Layer to Layer bHAST at 10 µm with dry desmear process 3.3 V (hour)		>200 hr
Within Layer bHAST at L/S = 9/12 µm comb (hour)		>200 hr
Regular hammer test without blistering/delamination	>20x reflow cycles	
Low rolled annealed copper solutions peel strength before/after HAST (kgf/cm)	>0.4	
Flame retardancy (Underwriters Laboratories 94)	V0	

Appendix A4: Additional/Summary Performance Requirements Met by PFAS-Containing ATPS Materials

Substrate core	Substrate buildup layer	Flux	Adhesives	Mold Compounds	Underfill	TIM
• Low-k (ε_r <2.94) • Ultra-low dielectric loss (tan δ <0.0008 at 10 GHz) • Low water absorption (<0.02%) • Low CTE (< 20 ppm/°C)	• Low-k (ε_r < 2.8) • Ultra-low dielectric loss • Low water absorption • Low CTE or CTE matching between EMC and pillars • High-strength adhesive • Improved dimensional stability • Compliance or e-matching between EMC and pillars • Improved surface-mount technology reliability • Plated through-hole reliability	• Diluent media • Cleaning agent • Base resin • Surfactant (0.01-1% by weight)	• Release agent • Pressure-sensitive adhesive • Chemical resistance • Flexibility • Bulk thermal properties	• Flame retardant • Dripping inhibitor • Catalysts • Resin thinner • Adhesive encapsulating gas barrier against water or steam • Fluorescent polymer compound	• Stress reduction • Semi-solid film formation	• High thermal conductivity • Tear resistance • High ultimate tensile strength (>5-10 Mpa) • High viscosity • Elastic

Appendix B: Description of Performance Requirements

Loss tangent and dielectric constant: Dielectric properties such a low dielectric constant (Dk) and loss tangent describe interactions of a dielectric material with an electric field. These two properties become more and more important for substrate materials as the semiconductor industry moves toward miniaturized circuits and high-speed and high-frequency applications.

The dielectric constant is the ratio of the permittivity of a material to that of free space and determines the relative speed at which an electrical signal traces in the material. The loss tangent is the ratio of the imaginary part of the dielectric constant to the real part and quantifies the dissipation of electrical energy caused by different physical processes such as electric conduction, dielectric relaxation and dielectric resonance.

Coefficient of thermal expansion (CTE): A material expands or shrinks upon heating. CTE quantifies the extent of thermal expansion – expect a negative value if the material shrinks when heated.

Glass transition temperature (Tg): Tg

Young's modulus: Young's modulus measures stiffness of a material under tension or compression. It is defined as the slope of the initial linear region of the stress-strain curve, where only elastic deformation occurs, and is reversible upon forceful removal of the material.

Fracture toughness (K_{IC}): KIC

Elongation at break: When a material is stretched, the length of the material along the direction of the tensile force increases. The ratio of the length increase of the material on breakage to the initial length is defined as the elongation at break. This term is a measure of a material's ductility. A material with too small elongation at break has a high tendency to forms cracks when subjected to the thermomechanical stresses present in the manufacturing processes and under operational conditions of final products.

Water absorption: Water absorption has negative impacts on the dielectric constant and reliability of a material, and is quantified using the percentage of water absorbed by a material relative to the dry mass of the material under specified conditions. The hydrophobicity of PFAS-containing materials help minimize water absorption and its negative impact on the dielectric constant and reliability of the material.

Peel strength: Depending on the deformation modes that a material may experience, it is possible to perform various tests to measure the adhesion strength between two materials. Peel strength is expressed as the average force per unit width of the bond line required to separate two bonded materials and can be measured based on American Society of Testing and Materials standard D3167.

