PFAS-Containing Wet Chemistries Used in Semiconductor Manufacturing

Semiconductor PFAS Consortium Wet Chemicals Working Group

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This publication was developed by the Semiconductor PFAS Consortium wet chemicals technical working group. The contents do not necessarily reflect the uses, views or stated policies of individual consortium members.

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About the Semiconductor PFAS Consortium

The Semiconductor PFAS Consortium is an international group of semiconductor industry stakeholders formed to collect the technical data needed to formulate an industry approach to perfluoroalkyl and polyfluoroalkyl substances (PFAS).

Consortium membership comprises semiconductor manufacturers and members of the supply chain, including chemical, material and equipment suppliers. The consortium includes technical working groups, each focused on the:

- Identification of PFAS uses, why they are used, and the viability of alternatives.
- Application of the pollution prevention hierarchy to (where possible) reduce PFAS consumption or eliminate use, identify alternatives, and minimize and control emissions.
- Development of socioeconomic impact analysis data.
- Identification of research needs.

This data will better inform public policy and legislation regarding the semiconductor industry's use of PFAS and will focus R&D efforts. The Semiconductor PFAS Consortium is organized under the auspices of the Semiconductor Industry Association (SIA). For more information, see www.semiconductors.org.

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Executive Summary

This paper identifies and describes the use of perfluoroalkyl and polyfluoroalkyl substances (PFAS) employed in the wet chemical processes used to manufacture advanced semiconductors. For the purposes of this discussion, PFAS includes chemicals with either a -CF2- or -CF3 moiety.

The category of wet chemical processes is a catch-all designation for almost all aqueous and organic liquid processing steps and is distinct from dry chemical processing steps like plasma etching and chemical vapor deposition (CVD). As such, wet chemical processes involve operations such as cleaning wafers before or after other process steps, applying chemicals to etch or plate wafers, and conducting chemical mechanical planarization (CMP).

Section 1 of this paper opens with a discussion on the use of PFAS in wet chemical processes and defines the concept of essential use as it relates to semiconductor manufacturing. Section 2 describes the methods to identify PFAS use in the industry. Section 3 summarizes advances in chip manufacturing and the challenges these advances pose on the manufacturing process. Sections 4 through 7 describe specific wet chemical operations, and why PFAS-containing materials are considered essential for each of them. Sections 8 through 10 address worker safety, environmental abatement and a substitution case example, respectively. Section 11 discusses topics of ongoing research and development.

Appendix A summarizes the terminology used to describe semiconductor manufacturing, which can be nuanced. Appendix B summarizes wafer processing challenges.

As demonstrated by the information collected and the physical and chemical requirements for advanced semiconductor manufacturing, it is clear that PFAS-containing materials provide a unique set of physical and chemical attributes that are essential for many semiconductor manufacturing processes. The industry and its suppliers have taken steps to eliminate the use of certain PFAS-containing materials; however, at

this point in time, suitable non-PFAS replacements have not been identified and tested for many wet chemical processes.

It is also important to include socioeconomic costs in regulatory agency deliberations concerning the manufacturing, use and disposal of PFAS-containing materials. The semiconductor industry has researched and will continue researching technologies to treat PFAS-containing wastewater from wet chemical operations.

1.0 Introduction

A number of applications across the semiconductor industry use fluorinated organic chemicals. Given the persistence, bioaccumulation and toxicity of some fluorinated organic chemicals, legislative and regulatory bodies worldwide are seeking to categorize a majority of fluorinated organic chemicals under a single class termed PFAS, and initiate restrictions that could limit the use of PFAS-containing materials to only those considered essential to the function of society.

This white paper is one in a series of 10 papers that seek to identify the principal applications of PFAS-containing materials, assess the application-specific performance requirements, and determine the role of fluorine in fulfilling performance requirements. The objective is to use this information to assess where the use of PFAS-containing materials in semiconductor manufacturing meets the definition of "essential" (Cousins, et al. 2019).

1.1 The Role of Wet Chemicals in Semiconductor Manufacturing

Wet chemical processing encompasses several different semiconductor fabrication processes, including wet chemical etching; planarization; electroplating; and wafer cleaning, rinsing and drying. Although these involve very different wafer processing operations with different objectives, the common factor is that they involve contacting a wafer with a liquid chemical mixture.

Wet chemical etching and cleaning operations typically occur in specialized "wets" tools that bring a liquid chemical mixture into contact with wafers, either by dispensing the mixtures onto a spinning wafer (in what are known as single-wafer wets tools) or by immersing one or more wafers into a tank for batch processing.

Wafer planarization occurs in CMP processes that dispense an aqueous chemical mixture containing abrasive particles. A pad helps provide continuous contact pressure between the CMP slurry and the rotating wafer surface.

Electroplating typically involves specialized wets tools that are equipped to apply a voltage potential across the liquid plating mixture and the wafer.

In most wet etch, CMP, electroplating and other wafer-cleaning operations, the areas of the wafer exposed to a wet chemical processing step are very specific regions defined by a photolithography masking operation. In assessing the complexity and challenge of conducting a wet chemical process, therefore, it is essential to consider the dimensions and geometric complexity of the integrated circuit features being fabricated. Although semiconductors are typically fabricated from crystalline silicon wafers that are generally either 200 mm or 300 mm in diameter and approximately 800-µm thick, the individual integrated circuit device structures often have critical dimensions measuring in nanometers and are thus at the molecular scale. The dimensions and material complexity of the device features – not the wafer as a whole – present challenges in wet chemical processing.

Figure 1 illustrates a relatively simple wet chemical etching operation where a patterned photoresist delineates the region of the wafer substrate on which the etchant operates. The etchant must transport into, react with and transport reaction product out of the region masked by the photoresist layer, while not stopping at nor removing material from the underlying substrate. The difficulty of the wet etch application generally increases with the need to etch features that are very narrow and deep and thus have a high aspect ratio. The difficulty of an etch operation also depends on the number and type of materials exposed to the etchant, and the relative removal rate for each material.

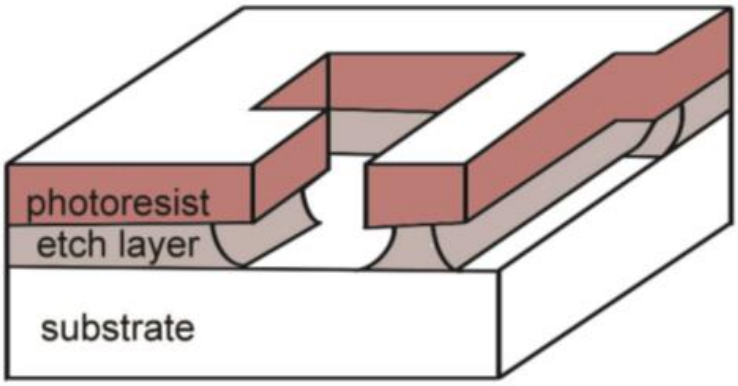

Figure 1: A conventional wet etch application.

1.2 Terminology

Describing the chemicals used to fabricate semiconductors into integrated circuits requires the use of some specialized terminology. This section defines a few of the terms that describe semiconductor devices and the process technologies used to fabricate them.

Integrated circuits, also known as computer chips, are fabricated from semiconductor materials, usually on a thin silicon wafer. The fabrication of a semiconductor occurs in specialized manufacturing facilities called fabs that cost between $5 billion and more than $20 billion, with 2,000 to 5,000 workers per fab. The clean rooms within which fabrication occurs provide an exceptional level of control against potential airborne molecular contamination, as described in the Occupational Exposure Controls section.

Transistors are the heart of integrated circuits, with a typical logic or memory chip containing 100 million or more transistors per square millimeter. It is necessary, therefore, to describe the dimensions of integrated circuits in units of nanometers. For instance, current-generation transistor gates are only a few nanometers wide, corresponding in size to only a dozen or so water molecule diameters (0.27 nm).

The fabrication of integrated circuits involves hundreds of individual repetitive additive and subtractive steps, each of which is patterned by a photolithography process, and many of which involve the use of wet chemical formulations. Here are the key terms to describe these processes; for additional detail, see Appendix A.

- Chemical formulation: A particular mixture of chemicals used to conduct a process step.
- Recipe: The specific composition, temperature, time, quantity and other process conditions used in a process step.
- Process step: An individual unit operation used to fabricate a wafer.
- Device structure: The individual geometric features that need fabricating in order to create an integrated circuit.

- Application: The specific combination of a chemical formulation and recipe within a process step used to achieve a desired state in a given device structure.

The composition of a wet chemical formulation and the recipe with which it is applied in a process step depend on the particular geometry and dimensions associated with the device structure. In this context, the need for fluorinated organic chemical ingredients may depend on the particular application-specific performance requirements. You may not need a PFAS surfactant in one application, but it may be essential for achieving the performance requirements in another application. For instance, you may not need a PFAS surfactant to etch a 100-nm diameter hole that is 200-nm deep (a 2-to-1 aspect ratio), but this surfactant may be essential for the etching of a 50-nm diameter hole that is 500-nm deep (a 10-to-1 aspect ratio).

It is useful to consider these definitions in the context of PFAS-containing materials and the essential use concept. The Semiconductor PFAS Consortium has defined the scope of PFAS-containing materials to include all chemicals that contain molecules with -CF2- and/or -CF3 moieties. As such, the consortium's definition closely aligns with the Organization for Economic Co-Operation and Development (OECD) definition (OECD 2021), although the OECD notes that "the term PFAS is a broad, general, nonspecific term, which does not inform whether a compound is harmful or not, but only communicates that the compounds under this term share the same trait for having a fully fluorinated methyl or methylene carbon moiety."

In fact, the application of the OECD definition lumps together gases, liquids and solids with vastly different properties that range in size from difluoromethane to large, highly complex organic polymers and surfactants. The absence of a unified, consensus definition for the term PFAS across regulatory agencies and legislative bodies is a complicating factor in the effort to document the uses and needs for fluorinated organic chemicals in wet chemical processing.

The essential use concept was first applied to ozone-depleting chlorofluorocarbons that were phased out under the Montreal Protocol except for certain "essential uses." Under this concept, essential uses are those "necessary for health, safety or critical for the functioning of society" where "there are no available technically and economically feasible alternatives" (United Nations 1987). Applying this definition of essential to PFAS-containing materials, as proposed by Cousins et al., the majority of PFAS uses in semiconductor manufacturing applications would be considered essential because semiconductors are critical for the functioning of society, and it is presently not possible to build semiconductors without the aid of numerous different types of PFAS-containing materials across a wide variety of semiconductor manufacturing applications (Cousins, et al. 2019). In many industries, including health care, transportation and defense, semiconductors serve a role where they are necessary for the health, safety and functioning of society. In a majority of semiconductor manufacturing processes, as well as in fabrication tools and infrastructures, there are no available technically or economically feasible alternatives to PFAS-containing materials, and as such their use is essential.

2.0 Methodology

In June 2022, consultants for the Semiconductor PFAS Consortium conducted a survey of consortium members, including semiconductor manufacturers, semiconductor equipment manufacturers and wet chemical suppliers. The purpose of the survey was to collect initial data on semiconductor PFAS use, in order to obtain a current industry and supplier understanding of PFAS use within wet chemical formulations and the criticality of PFAS-containing materials within wet chemical formulations and processes. The consultants compiled the results and removed company-specific information to achieve anonymity.

The survey asked respondents to reply for all semiconductor manufacturing facilities, equipment and chemical formulations within their company; thus, responses are not specific to a single geography. For the purposes of the surveys, the term "use" means to procure, employ or consume a chemical or material and does not imply the generation, development, production and/or importing for the purpose of redistribution (including producing formulations). The results of the survey are limited to the knowledge and manufacturing operations of participating Semiconductor PFAS Consortium members. Additional wet chemical uses of PFAS outside those surveyed may exist. Although the survey responses listed do not represent the entirety of the semiconductor wet chemical supply chain, the data is based on input from many of the principal wet chemical and process equipment suppliers and semiconductor device makers.

Table 1 lists the wet chemical process survey results for 28 different wet chemical formulations. Roughly half of these formulations are listed with specified compositions. Others are described generically, with names like aqueous and nonaqueous surface modification treatment, nonlithographic coatings, and oxide or metal CMP slurry. The use of generic formulation names is indicative of the wide breadth of chemical formulations used in wet chemical formulations, many of which are proprietary.

Several responses indicated that the device maker did not know whether a PFAS-containing material was present in a formulation. This reflects different practices across the semiconductor industry, where some companies require that a supplier fully disclose every formulation, usually under a nondisclosure agreement that limits distribution of the composition information to environmental, safety and health personnel. Device makers that do not have this requirement would only know the composition of a formulation to the extent that it is listed on a safety data sheet (SDS), which is limited to nonproprietary components.

In 16 (57%) of the formulations, respondents indicated that there was no PFAS component. Primarily, these formulations consist of a simple acid or base in water. For nine (32%) of the formulations, respondents indicated production both with and without a PFAS component. This result indicates that many formulations are application-specific and vary depending on the particular products being produced by the device maker. Buffered hydrofluoric acid (BHF), for instance, is supplied both with and without a surfactant because not all applications using BHF require it. As described in the next section, the need for a surfactant to be fluorinated or not depends on the application-specific performance requirements, including the geometry of the specific device structure being etched, cleaned or dried.

Table 1: Semiconductor wet chemical process steps and formulations evaluated based on Semiconductor PFAS Consortium member survey responses.

Process Step	Formulation Evaluated	Presence of PFAS-Containing Material[3]	PFAS Component Unknown[4]	No PFAS-Containing Material Identified[5]
Etch/Clean	Standard Clean (SC1/APM)[1]			X
Etch/Clean	Standard Clean (SC2/HPM)[2]			X
Etch/Clean	Sulfuric Acid with Peroxide (Piranha)			X
Etch/Clean	Tetra Alkyl Ammonia Hydroxides			X
Etch/Clean	Phosphoric Acid			X
Etch/Clean	Acetic Acid			X

Process Step	Formulation Evaluated	Presence of PFAS-Containing Material[3]	PFAS Component Unknown[4]	No PFAS-Containing Material Identified[5]
Etch/Clean	Nitric Acid			X
Etch/Clean	Sulfuric Acid			X
Etch/Clean	Hydrogen Peroxide			X
Etch/Clean	Ammonium Hydroxide			X
Etch/Clean	Liquid Hydrofluoric Acid			X
Etch/Clean	Liquid Hydrochloric Acid			X
Etch/Clean	Aqueous Backside Cleaning for Extreme Ultraviolet (EUV)			X
Etch/Clean	Organic Backside Cleaning for EUV			X
Etch/Clean	CMP Post-Cleans		X	
Etch/Clean	BHF Used in Buffered Oxide Etch (BOE)	X		X
Etch/Clean	Organic-Based Etch	X		X
Etch/Clean	Organic-Based Clean	X		X
Etch/Clean	Organic Clean for Semiconductor Equipment and Components	X		
Etch/Clean	Post-Plasma Etch Photoresist Strip	X		X
Etch/Clean	Aluminum Etch (Phosphoric Acid/Nitric Acid/Acetic Acid)	X		X
CMP	Oxide CMP Slurries	X		X
CMP	Metal CMP Slurries		X	X
Surface Modification Treatment (SMT)	Organic SMT Formulations	X	X	X
SMT	Aqueous SMT Formulations	X	X	X
Coatings	Nonlithography Organic Coatings	X	X	X
Plating				X
Backgrind				X

[1]SC1 or APM is a mixture of ammonium hydroxide (28 wt%), hydrogen peroxide (30 wt%) and water.
[2]SC2 or HPM is a mixture of hydrochloric acid, hydrogen peroxide and water.
[3]At least one respondent indicated the presence of a PFAS-containing material in at least one fab.
[4]At least one respondent indicated that they did not know whether a PFAS-containing material was present.
[5]At least one respondent indicated that PFAS-containing materials are not present in these formulations.

3.0 Wafer Processing Challenges

Semiconductor technology has undergone rapid and dramatic advances. In 1984, the transistor gate dimension was on the order of 5 micrometers (µm) to 7 µm, with advanced chips containing more than 2,000 transistors per square millimeter (Wikipedia Contributors 2023). In 2023, the critical dimensions of advanced transistor gates are on the order of just a few nanometers, with advanced chips containing more than 300 million transistors per square millimeter.

The advances in chip density have been accomplished with the shift from conventional planar architectures to the third dimension. Figure 2 illustrates an increase in geometric complexity. Appendix B includes additional descriptions of semiconductor manufacturing technologies.

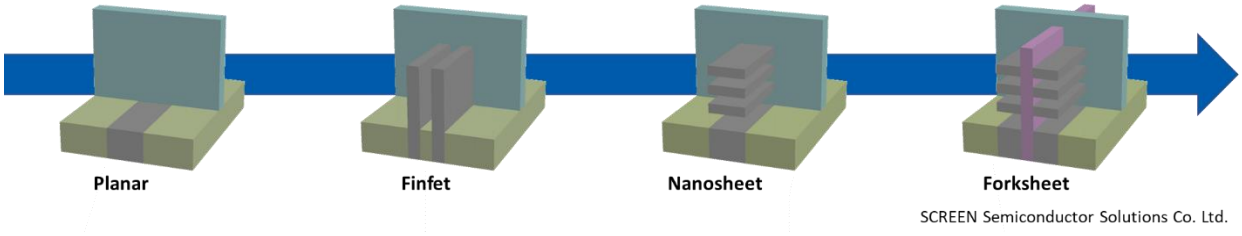

Figure 2: The evolution of device architectures over time. In addition to the increasing geometric complexity, the size of critical dimensions has decreased and transistor density has increased (Brown 2022).

In addition to the shift to three-dimensional geometries, the physical dimensions of the features that must undergo wet chemical processing are continuously pushing new extremes. At the 7-nm technology node, for instance, device structures may be only 8-nm wide. The holes between fins may be 4-nm-by-8-nm wide and 60-nm deep (Vereecke, De Coster, et al. 2018); (Collaert 2022).

The geometric complexity and physical dimensions of memory chips have also undergone dramatic advances, as illustrated in Figure 3, where there may be 200 or more stacked layers in a 3D not-and (NAND) flash memory, with each layer only 25-nm thick and yet 4,000-nm deep (Park, et al. 2023); (Zhou, et al. 2023).

Vertical NAND cells are fabricated from stacked silicon nitride/silicon dioxide layers by a CVD process, followed by the vertical punching of through-holes by dry etching, and the selective removal of silicon nitride by wet chemical etching. Deep contact holes in 3D NAND memory may have aspect ratios of 60 or higher (Cho, et al. 2022).

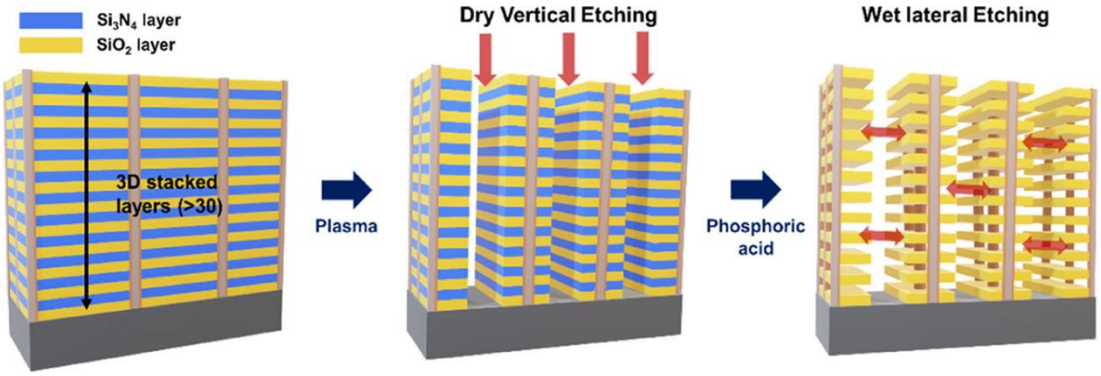

Figure 3: 3D NAND flash memory manufacturing process and wet lateral etching. Each nitride layer is 25- to 40-nm thick and 4,000-nm deep (Lee, et al. 2021).

The challenges in wet etching a silicon nitride/silicon dioxide paired-layer 3D NAND multistack structure are representative of the continuing innovations required of aqueous etch formulations. In particular, the extreme aspect ratio and requirement for materials selectivity present challenges that require continued innovation in the development and use of additives to supplement the action of wet chemical formulations.

4.0 Conventional Aqueous Wet Clean and Etch Operations

The sequence of manufacturing steps used to fabricate semiconductors includes ubiquitous and repetitive aqueous etch and clean process steps. At a high level, the wet clean processes applied to a wafer include removing (Peethala, et al. 2023):

- Organic and metallic particulates and contaminants.
- Unreacted residue following film deposition.
- Residues from plasma etching steps.
- Organic and metallic contaminants from its back side or beveled edges.

Applying wet etch processes to wafers (Peethala, et al. 2023):

- Removes materials such as dielectrics, metals, organics, metal nitrides and anti-reflective coatings.
- Etches or recesses a variety of materials, including metals, dielectrics, oxides and silicon to achieve targeted geometries.

As noted, many aqueous etch and clean formulations comprise relatively simple mixtures of acids or bases that in some cases may contain an oxidizing agent or other additive, as summarized in Table 1.

For each wet chemical formulation, there are many different performance attributes that depend on the particular process step during which the formulation is applied, and the particular device structure being fabricated. The performance requirements are therefore application-specific. For example, a wet etch process known as a post-etch residue remover (PERR) applied in a 0.25-µm upper metal layer with features 1-µm wide has very different requirements than a PERR applied to a modern dynamic random access memory bit line with feature sizes <10 nm. Similar disparities exist in the cleaning of legacy device structures such as those associated with >90-nm logic technologies vs. cleaning the channel in a 376-layer 3D NAND memory structure with a 25-nm channel width and a 4,000-nm channel depth.

The majority of the aqueous clean and etch formulations listed in Table 1 consist of acidic and basic formulations used in cleaning and etching steps and do not use a PFAS additive. These formulations include dilute hydrofluoric acid (DHF) containing 0.1 to 0.5% hydrofluoric acid; dilute sulfuric acid (DSP) containing hydrogen peroxide; hydrochloric acid (5% or lower in conjunction with hydrogen peroxide, also known as HPM or SC2); and phosphoric acid (~88%). Some back-end-of-line (BEOL) cleaning steps may use DHF with a very low level of dissolved oxygen to clean structures with exposed copper. Semiaqueous formations used for BEOL cleaning often contain a fluoride salt and hydrofluoric acid.

Common basic formulations include those based on ammonium hydroxide or tetramethylammonium hydroxide (TMAH). A mixture of ammonium hydroxide (28 wt%), hydrogen peroxide (30 wt%) and water, known as APM or SC1, has long been the workhorse for cleaning silicon and dielectric materials, especially for removing particles. Historically, APM has been formulated in a NH_4OH-to-H_2O_2-to-H_2O

ratio of 1-to-1-to-5, whereas many current applications use a more diluted version of APM such as 1-to-1-to-100. Using surfactants and applying a megasonic field enhances particle removal efficiency in APM processes. However, based on consortium surveys, PFAS additives are not used in APM processes.

The predominant uses of TMAH-based formulations in wet clean and etch processes are for polysilicon etching and anisotropic etching of silicon for through silicon via (TSV) and to create micro-electromechanical systems (MEMS) structures. Unlike NH_4OH, TMAH does not attack copper aggressively, and thus works well in cleaning copper-containing structures. TMAH-based formulations are also used in photoresist development (Ober, Kafer and Deng 2022). Aqueous TMAH used as a photolithography developer often employs a surfactant; however, based on consortium surveys, PFAS additives are not used in TMAH-containing formulations.

4.1 BHF

BHF, also known as BOE, is an aqueous etchant used in the fabrication of semiconductors. BHF has historically been associated with the selective etching of silicon dioxide from silicon surfaces, and the etching of silicon nitride. It is also used in a wide variety of other applications, however, including the etching of contact holes and photoresist stripping.

BHF consists of an aqueous mixture of hydrofluoric acid and ammonium fluoride, and sometimes employs a surfactant. Adjusting the proportion of hydrofluoric acid and ammonium fluoride in a particular BHF mixture in turn adjusts the pH and active chemical species in order to suit the device-dependent needs of a particular etching operation. Adding surfactants to some BHF formulations facilitates wetting, penetration and mass transport. Perfluorooctyl sulfonate (PFOS) was used as a surfactant in BHF formulations, but was eliminated and replaced with alternative surfactants, as described in the Substitution Example section.

The product data sheet for 3M™ Electronic Surfactant 4200 and its associated SDS (3M 2020); (3M 2022) describe one known alternative to PFOS in BHF applications. The product data sheet describes the product as an additive designed to improve wetting in BHF or BOE solutions in semiconductor, flat-panel display and solar panel applications (3M 2020). The SDS lists the active ingredient as 1-Butanesulfonamide, 1,1,2,2,3,3,4,4,4-nonafluoro-N-(2-hydroxyethyl)-, ammonium salt (1-to-1) (3M 2022). See Figure 4.

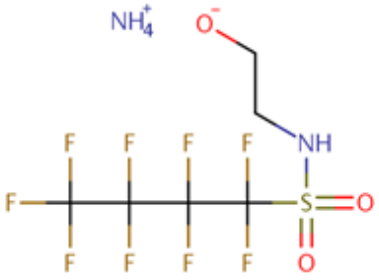

Figure 4: Chemical structure of butanesulfonamide, 1,1,2,2,3,3,4,4,4-nonafluoro-N-(2-hydroxyethyl)-, ammonium salt (1-to-1).

BHF formulations are used to wet etch or clean a variety of different wafer substrate materials, including silicon, polysilicon, silicon oxide, silicon nitride, aluminum, copper and photoresists. The challenge in conducting these operations varies greatly depending on the juxtaposition of materials and the geometric complexity of the feature being etched. One common application of BHF is the removal of silicon dioxide

from a silicon surface. Another application involves the etching/cleaning of contact holes, which can vary significantly in their critical dimensions and aspect ratios.

In some BHF applications, the use of a surfactant is necessary to perform the etch or clean operation successfully. Applications driving the use of a surfactant include the need to:

- Facilitate fluid entry of the BHF into – and reaction products out of – a capillary space by reducing the surface tension of the fluid and the contact angle with the solid (Miyamoto and Gotoh 1998).
- Adsorb to a surface to prevent the deposition of metals introduced into the solution during an etching process (Ohmi, et al. 1992).
- Mitigate the formation of air bubbles that can form and cause failure during the BHF etching of contact holes (Shimizu and Iwakuro 1996).
- Adsorb to a surface to suppress etching of one material while preferentially removing another material. For instance, in the removal of silicon dioxide from the surface of a silicon substrate, a surfactant is employed to selectively adsorb to the silicon surface and suppress its etching while the silicon dioxide is removed (Kikuyama, et al. 1990); (Miyamoto, Kita, et al. 1994).

The selection of a particular surfactant for one of these applications varies depending on the application-specific requirements. Important factors that can drive a requirement for a fluorinated surfactant include:

- If the surfactant must resist decomposition under chemically reactive conditions, including acidic, basic, oxidizing or reducing conditions. Fluorocarbons have the strongest bonds known in organic chemistry.
- If the mixture must achieve very low surface tensions or contact angles. Fluorinated surfactants can achieve lower aqueous surface tensions (15 to 20 millinewtons per meter) than hydrocarbons (~30 mN/m) and other known materials, including fluorosilicates. This is because fluorinated surfactants have low polarizability, a high molecular surface area and the molecular conformation of the perfluorocarbon tail groups.
- If the surfactant must retain its surface activity at a very low pH. Fluoroalkyl acid surfactants, for instance, typically have near-zero acid dissociation constant (pK_a) values; therefore, their headgroup remains ionized and hydrophilic even if the pH approaches zero.
- If the surfactant must be surface-active in a nonaqueous media. Surfactants with perfluorinated tail groups are oleophobic as well as hydrophobic.

In many applications, several if not all of these factors together are essential to the performance of a fluorinated surfactant. For instance, it may not be solely that a fluorinated surfactant has a lower surface tension, a lower pK_a or is more resistant to oxidation, but rather simultaneous attributes that enable the surfactant to perform for the application.

One nonfluorinated surfactant used in some BHF formulations is the alkylphenol polyglycidol nonionic Olin Hunt surfactant (OHS), supplied by Olin Microelectronic Materials (Almanza-Workman, Raghavan and Sperline 2000). See Figure 5. The ability of a nonfluorinated alternative to serve as an alternative depends on the application-specific performance requirements.

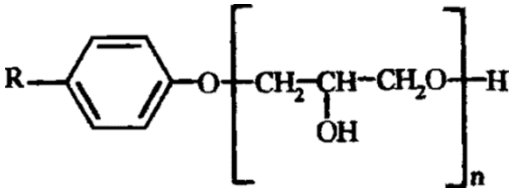

Figure 5: The chemical structure of OHS, an alkylphenol polyglycidol nonionic surfactant.

4.2 Organic-Based Etch and Clean Solutions

In some etch and cleaning applications, the substrate materials are not tolerant of water or oxygen, and consequently require an organic-based formulation. For instance, germanium is susceptible to rapid oxidation that degrades electrical performance because germanium oxides contain many defects; therefore, an organic acid-based etchant may provide the best performance (Heslop and Muscat 2019).

In other cleaning applications, an organic material is present on the wafer substrate, and only an organic solvent-based formulation can provide the necessary penetration and solvation needed to remove the material. The removal of photoresist and bottom anti-reflective coating from a wafer surface, in a wet chemical operation known as photoresist strip, often requires an organic solvent-based wet chemical formulation (Le, Claes, et al. 2009). It may be particularly difficult to remove the fluorocarbon polymer residuals that remain from plasma etch processing, thus requiring the solvating properties of an organic-based formulation (Le, de Marneffe, et al. 2011); (Thanu, Raghavan and Keswani 2011).

The survey conducted by the Semiconductor PFAS Consortium indicated that some companies employ fluorinated organic solvent-based etch and clean formulations. Without specific formulation compositions or applications, we have only limited information on their use and the application-specific performance factors that might drive the use of a PFAS compound. In general, a fluorinated organic solvent might be needed where an inert, nonflammable solvent with specified polarity and solvency properties are required. Adding reactive moieties or ingredients to the organic formulation might endow the mixture with additional performance characteristics.

4.3 Post-Plasma Etch Photoresist Strip

A number of etching applications use a fluorinated gas plasma etch process known as reactive ion etch (RIE) or plasma etch. Plasma etch processes create a fluorinated polymer film on the sidewall of an etched feature to help keep the sidewall open and plumb. The residual fluorinated film may be on the order of tens of angstroms thick and is typically removed using a combination of a dry etch with an oxygen plasma and a wet chemical clean (Seo, et al. 2002). Additionally, the photoresist used to mask adjacent areas is chemically and physically altered by plasma etching, and requires a wet chemical process for etch residue removal. In some applications, these wet chemical formulations may contain proprietary fluorinated components.

4.4 Aqueous Aluminum Etch

Formulations comprising an aqueous mixture that includes phosphoric acid, nitric acid and acetic acid are sometimes referred to as aluminum etch and may employ a PFAS-containing material or another surfactant. Although referred to as aluminum etch, uses for etching other metals are often reported. Consortium survey respondents did not describe the specific performance requirements driving the use of a fluorinated surfactant in metal etching applications, but these requirements may be similar to those described earlier for certain BHF formulations.

5.0 High-Aspect-Ratio Collapse Mitigation Materials

A critical challenge in semiconductor processing is the pattern collapse of nanostructures with hydrophilic surfaces during drying steps. This collapse occurs during the patterning of structures containing high-aspect-ratio photoresist lines as well as during the fabrication of certain types of structural features such as memory devices, which contain tall cylindrical silicon capacitors or nanosheets.

Pattern collapse is a critical yield issue in integrated circuit manufacturing, and with the increasingly smaller and more narrowly dimensioned device structures associated with advanced technology nodes, is

becoming increasingly difficult. Mitigating line collapse issues requires innovative chemical formulations, including formulations that use PFAS-containing materials.

The collapse occurs when the capillary forces created by liquid menisci formed between high-aspect-ratio features exceed the structural strength of the material forming the walls of the capillary space. In the case of a liquid with surface tension γ_L making a contact angle of θ on the walls of two structures separated by distance d, Equation 1 gives ΔP, the collapse pressure (also known as the Laplace or capillary pressure), also illustrated in Figure 6:

$$\Delta P = 2\,\gamma_L \mathrm{Cos}\,\theta / d \qquad (1)$$

As Equation 1 infers, it is possible to reduce the capillary force by reducing the value of $2\,\gamma_L \mathrm{Cos}\,\theta$. This value is directly proportional to the surface tension, and as noted earlier, the surface tension achievable with fluorinated surfactants is substantially lower than what alternative chemicals can provide. The Semiconductor PFAS Consortium white paper, "Background on Semiconductor Manufacturing and PFAS," describes the molecular attributes that allow fluorinated surfactants to achieve much a lower surface tension than alternative chemicals.

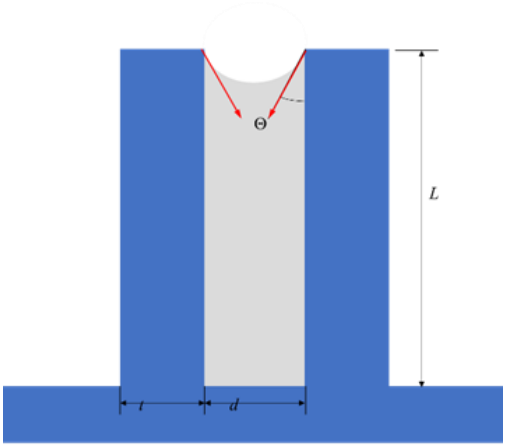

Figure 6: The collapse of two vertical lines connected by a wetting liquid.

First reported during MEMS fabrication, pattern collapse occurred again during the patterning of submicron photolithography features, and subsequently with the fabrication of increasingly complex and finer geometries associated with advanced memory and logic features (Bassett 2019); (Gale 2018). Steps to mitigate pattern collapse initially centered on the use of low-surface-tension liquids like isopropanol (IPA), followed by actions that change the contact angle, and subsequently more elaborate means of eliminating surface tension forces entirely (Bassett 2019); (Gale 2018).

Almost all advanced semiconductor fabrication facilities use some version of hot IPA drying to remove water from wafer surfaces and mitigate the influence of capillary forces, as illustrated in Figure 7. The surface tension of aqueous IPA is limited to about 27 mN/m at room temperature. Thus, fluorocarbons, which have much lower surface tensions (~15 mN/m), are sometimes used as alternatives to IPA. For example, methoxy nonafluorobutane ($C_4F_9OCH_3$) provides performance characteristics that can replace IPA in surface-tension gradient systems for wafer drying. Unlike IPA, these types of fluorinated fluids are nonflammable and can dry resist-coated wafers without damaging the resist.

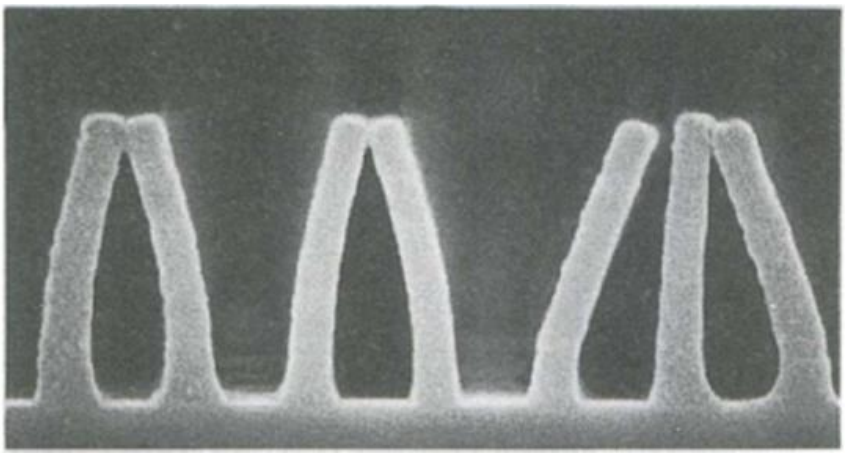

Figure 7: The collapse of photoresist lines by capillary forces (Bassett 2019).

Another approach to mitigate pattern collapse issues is a technique known as surface modification. In this technique, formulations provide a water-repellent surface by reacting with the underlying substrate to create a hydrophobic coating on vulnerable features. The hydrophobic coating modifies the contact angle and forces associated with the interaction of the surface of the semiconductor features with wet cleaning agents.

In addition to mitigating pattern collapse caused by capillary forces, reducing the contact angle helps mitigate pattern collapse caused by the adhesive forces between adjacent pillar structures (Bassett 2019). Surface modification techniques include the use of self-assembled monolayers (SAMs) of long-chain alkanes and the use of a fluorinated silane SAM, among others (Maboudian, Ashurst and Carraro 2000); (Ghosh 2022). Unfortunately, compounds used in SAM techniques are easily hydrolyzed, and thus require organic solvents.

Additional alternatives include the processes of supercritical carbon dioxide drying, sublimation drying, sacrificial gap fill with a polymer solution followed by solidification and dry ashing, or using a hydrocarbon-based rinse agent that can make the surface hydrophobic through acid-base interactions. There are advantages and disadvantages to each of these alternatives.

In supercritical drying methods like those that use supercritical carbon dioxide, the liquid is heated and pressurized into a supercritical fluid state. Purging the device feature with the supercritical fluid (Bassett 2019) dries the wafer. The main issue with this technique is that it does not allow high wafer throughput.

In sublimation drying, a liquid, such as tert-butyl alcohol, is first frozen to a solid and then further cooled and decompressed below the triple point, followed by heating to sublimate the solid directly to a vapor (Bassett 2019); (Watanabe, et al. 2013). Sublimation drying and supercritical drying both have logistical and infrastructure difficulties associated with high-pressure cryogenic processing (Bassett 2019).

The sacrificial polymer gap fill method involves dispensing a polymer solution to displace the rinse liquid, followed by polymerization to form a solid polymer in the channels and thus provide mechanical support and prevent pattern collapse. Dry ashing or thermal decomposition subsequently removes the solid polymer (Varaprasad, et al. 2018); (Drage 1999).

When PFAS-containing surface modifiers, polymer chemistries or hydrocarbon-based rinse agents generate a solvent-based waste stream, these chemistries are typically collected and disposed of using high-temperature waste incineration facilities.

6.0 CMP and Post-CMP Cleans

CMP is a semiconductor manufacturing process that uses water-based slurries comprising mixtures of abrasive particles (silica, alumina or ceria) with chemical components such as acids, bases, oxidizers, chelating agents, metal passivating agents, surfactants or other control agents to remove a wide range of film types (silicon dioxide, silicon nitride, tungsten, copper) (Krishnan, Nalaskowski and Cook 2010). CMP accomplishes this through the combined action of chemical and mechanical forces.

CMP slurries and post-CMP cleaning solutions routinely use surfactants. In slurries, surfactants may disperse the particles, improve slurry stability, control the wettability of films and polishing pads, and reduce the corrosion of some films (Krishnan, Nalaskowski and Cook 2010). Since the duration of the CMP process is short (tens of seconds to a couple of minutes), the surfactants must ideally exhibit rapid adsorption on films during polishing, and rapid desorption during water rinsing following the CMP polishing steps. The surfactants should be nonfoaming to prevent foaming during mixing, handling and CMP.

PFAS surfactants can lower the surface tension of aqueous solutions to low values (down to ~20 mN/m) rapidly, can be tailored to be nonfoaming, and can resist degradation by reactive oxygen species produced in oxidizing systems. Although only used in very specialized instances, certain types of CMP slurries for targeted performance improvements do include fluorinated surfactants because of their ability to enable selective film inhibition and the wetting of low-surface-energy substrates.

Post-CMP cleaning formulations may include a range of chemistries, such as chemicals for controlled mild etching; reagents to remove particulate and metallic contamination; and corrosion inhibitors, especially for galvanic corrosion between exposed metallic materials. Commercial p-CMP cleaning formulations include many types of nonionic hydrocarbon surfactants, such as alkyl polyethylene oxide alcohols and ethoxylated acetylenic alcohols. Some p-CMP cleans may contain fluorinated organics.

7.0 Metal Plating

Semiconductor wafer manufacturing and post-fabrication packaging include a variety of electrolytic and electroless plating operations. Plating solutions commonly contain surface-active components. However, the results of the Semiconductor PFAS Consortium survey did not indicate any current uses of PFAS-containing materials in metal plating.

In consideration of the use of surfactant components in plating formulations, this section summarizes the utility and potential future applicability of PFAS-containing surfactants.

In plating solutions, surfactants:

- Reduce surface tension to improve wetting and allow the plating bath solution to access geometric features with high aspect ratios.
- Reduce surface tension to allow the release of hydrogen gas generated at electrodes, rather than allowing the gas to deposit into the metal (Dubin, et al. 1997).
- Reduce surface tension to reduce bubble size and mitigate acid mist formation.

In addition to conventional plating operations, the electroless plating of copper is conducted in trench/via fill operations, and sometimes requires a surfactant to prevent interference from hydrogen, which is generated as a byproduct. While Dubin et al. describe the potential use of alternative nonfluorinated surfactants in electroless plating operations, efficacy under manufacturing conditions is unknown (Dubin, et al. 1997).

Table 2 summarizes principal applications of PFAS in wet chemicals processing.

Table 2: Principal applications of PFAS-containing materials in semiconductor wet chemical processing.

PFAS use area	Role of PFAS additives	Concern of alternative	Criticality for semiconductor devices manufacture
Aqueous etch/clean formulations Organic-based etch formulations	Facilitate entry of the wet etchant into - and reaction products out of - a capillary space by reducing the surface tension of the fluid and the contact angle with the solid. Adsorb to a surface to prevent the deposition of metals that are introduced into the solution during an etching process. Mitigate the formation of air bubbles. Adsorb to a surface to suppress etching of one material while another material is preferentially removed.	The surface-active agent must resist decomposition under chemically reactive conditions. Fluorinated surfactants can achieve lower aqueous surface tensions (15 to 20 mN/m) than hydrocarbons (~30 mN/m) and other known materials including fluorosilicates. Fluoroalkyl acid surfactants have uniquely low pK_a values that enable them to remain ionized and hydrophilic even if the pH approaches zero. Surfactants with perfluorinated tail groups are oleophobic as well as hydrophobic, and therefore are surface active in organic solvents as well as aqueous etchants.	PFAS additives are critical for some, but not all wet etch applications. The requirement for a PFAS additive depends on the physical dimensions and aspect ratio of the device feature being etched and the particular set of materials exposed to the etchant during etching.
CMP	Surfactants and surface-active materials are critical components of CMP slurries and post-CMP cleaning solutions. These components must: • Disperse the particles. • Provide slurry stability. • Control the wettability of films and polishing pads. • Reduce corrosion of some films. Fluorosurfactants are critical to achieving CMP performance requirements in certain situations. In particular, they enable selective film inhibition	The surface-active agents must rapidly adsorb to the substrate during polishing and rapidly desorb with water rinsing and must be nonfoaming. In situations requiring a very low surface tension, only PFAS surfactants can lower the surface tension of aqueous solutions to values below ~20 mN/m rapidly. In chemically aggressive CMP formulations, a PFAS surface-active agent may be necessary to prevent degradation by reactive	PFAS additives are critical for some but not all CMP applications. The requirement for a PFAS depends on the material properties of the exposed surfaces that need protection, surface tension reduction requirements and the aggressiveness of the CMP formulation.

PFAS use area	Role of PFAS additives	Concern of alternative	Criticality for semiconductor devices manufacture
	and the wetting of low-surface-energy substrates.	oxygen species produced in oxidizing systems.	
Organic solvent-based clean formulations	Some wafer clean/strip formulations and cleaning operations conducted on parts outside of fab clean rooms require organic solvents. In some applications, these mixtures comprise fluorinated organic solvents and/or fluorinated organic alternatives in order to provide the necessary solvency and fluid-handling characteristics.	The ability of a solvent to dissolve and solubilize a material from the surface of a wafer or part depends on its respective chemical characteristics, as often represented by the Hansen solubility parameters (dispersion, polar and H-bonding intermolecular forces). In some cases, therefore, a fluorinated component is necessary to remove fluorinated materials from a surface.	PFAS-containing solvent mixtures are critical for some but not all solvent clean applications. The requirement for a PFAS depends on the material properties of the substance that needs removing.
Pattern collapse mitigation	PFAS-containing materials are used in a number of different formulations that are used to mitigate pattern collapse issues, including surfactants, surface modification treatment materials, displacement fluids and organic solvents. Historically associated with photoresists, pattern collapse is now a critical and evolving challenge in the etching and drying of narrow-dimensioned, high-aspect-ratio device features like nanosheets and 3D NAND structures. Pattern collapse occurs when the capillary forces created by liquid menisci formed between high-aspect-ratio features exceed the structural strength of the material forming the walls of the capillary space.	The ability of a non-PFAS alternative to serve effectively as a means of pattern collapse mitigation depends on the particular application. Several different approaches are in use or being pursued as a means of mitigating pattern collapse issues that are evolving with the increasing use molecular dimension device structures.	Some PFAS-containing formulations used to mitigate pattern collapse may be essential. The development of new solutions for the evolving pattern collapse issue may be able to avoid the use of fluorinated organics depending on the application-specific performance requirements.
Plating and electroplating	Plating and electroless plating use surfactants and surface-active materials to: • Reduce surface tension to improve wetting and access to the plating bath solution to geometric features with high aspect ratios.	The surface-active agent must resist decomposition under chemically reactive conditions, particularly at plating electrodes. Fluorinated surfactants can achieve lower aqueous surface tensions (15 to 20	PFAS-containing plating mixtures are critical for some but not all plating applications. The requirement for a PFAS is application-specific and therefore depends on the material properties of

PFAS use area	Role of PFAS additives	Concern of alternative	Criticality for semiconductor devices manufacture
	• Mitigate the inclusion of hydrogen gas generated at electrodes. • Mitigate bubble and/or mist formation.	mN/m) than hydrocarbons (~30 mN/m) and other known materials including fluorosilicates. Fluoroalkyl acid surfactants have uniquely low pK_a values that enable them to remain ionized and hydrophilic even if the pH of the plating solution approaches zero.	substance being plated, as well as the dimensions and aspect ratio of the features being plated.

8.0 Occupational Exposure Controls

Fabs employ a hierarchy of design features that isolate workers and wafers from chemicals and contaminants. For an extensive description of the design and operating practices that protect employees from chemicals, see the Semiconductor PFAS Consortium white paper, "Background on Semiconductor Manufacturing and PFAS."

9.0 Environmental Releases and Controls

Semiconductor fabs generate organic and aqueous waste streams that are treated in accordance with local and federal waste and wastewater regulations, typically collecting and disposing of organic waste as a blended fuel through high-temperature incineration or reprocessing. For more detail, see the Semiconductor PFAS Consortium white paper, "Background on Semiconductor Manufacturing and PFAS."

Historically, the majority of aqueous chemicals employed in semiconductor manufacturing processes are discharged to an industrial wastewater drain system that conveys wastewater for the treatment of specific regulated pollutants in accordance with local and federal regulations, with subsequent discharging to a publicly owned treatment works (POTW) or surface water. Most PFAS are not regulated pollutants; therefore, unless company-specific provisions are in place, wastewater from processes that use aqueous wet chemical formulations that contain PFAS would likely be discharged to the POTW without substantive removal of the PFAS.

Given the rapidly evolving environmental and health concerns associated with PFAS, many companies are evaluating their PFAS discharge by conducting material balance and/or by analyzing and instituting chemical management and wastewater treatments to minimize the discharge of PFAS.

The industry is actively researching PFAS wastewater releases and treatment technologies, as described in the Semiconductor PFAS Consortium white paper, "Background on Semiconductor Manufacturing and PFAS."

10.0 Substitution Example

This substitution example summarizes the actions taken by a device maker from 2002 to 2009 to replace PFOS surfactants from certain BHF etch applications with a four-fluorocarbon surfactant based on a perfluorobutanesulfonic acid moiety.

The first stage of the chemical substitution effort took approximately four years and involved collaborations between company and supplier chemists and engineers to identify several potential replacements for evaluation. The second stage involved qualifying the identified alternative and implementing it on manufacturing lines in the company's 200- and 300-mm fabs.

In total, the device maker eliminated PFOS from approximately 100 BOE operations across 1,000 different products in over 50 different technologies, reducing the total amount of PFOS in its BHF applications from approximately 187 pounds per year in 2006 to zero by the end of 2009. The replacement for PFOS, an eight-perfluorocarbon chain surfactant, was a four-fluorocarbon chain analog; at the time, both the U.S. Environmental Protection Agency and the supplier deemed the replacement safe and prudent. The replacement of PFOS with a shorter-chain analog required a phased approach, involving dozens of research and engineering personnel over an 8-year period. The company received a State Governor's Award for Environmental Excellence and Pollution Prevention for the elimination. However, the implemented alternative is now considered a regrettable substitute.

In comparison to an eight-year effort to identify and qualify a shorter-chain perfluorinated analog, the identification and qualification of an alternative surfactant that does not employ -CF2- or -CF3 moieties (if viable) would be significantly more challenging, and could take more than the eight years required for the PFOS replacement.

11.0 Research and Development Needs

Potential areas of research and development to identify alternative materials and processes and continue to advance the protection of human health and the environment include the development of:

- Nonfluorinated surfactants that provide the necessary functionality for wet chemical cleaning and etching operations, and that are also environmentally benign, or at least readily amenable to conventional wastewater treatment or recycling processes.
- Alternative methods for mitigating pattern collapse that use environmentally benign materials and processes. Currently researched options, like supercritical carbon dioxide and gap fill methods, have limited viable high-volume manufacturing applications and require improvements.
- Alternative semiconductor manufacturing processes for wet chemical applications that are inherently more benign and exert less resource demand on the overall semiconductor manufacturing process ecosystem.
- Waste and wastewater control technologies that cost-effectively separate PFAS-containing materials from wet chemical waste streams, and either recycle or destroy these materials by mineralization.
- Improved chemical analytical methods and metrology to manage PFAS wastes, effluents and emissions. There are validated and commercially available analytical methods for fewer than 100 of the thousands of PFAS-containing materials used in commerce or found in the environment.
- Improved predictive and analytical methods for chemical properties, behavior and toxicity.

12.0 Timelines

The timeline needed to develop, qualify and implement alternatives falls into four broad categories:

- **Three to four years.** If an existing non-PFAS alternative is available, does not require infrastructure alterations, and demonstrates adequate performance for a specific application, then it typically takes three to four years to conduct the trial testing and implement the alternative into high-volume manufacturing.

- **Three to 10-plus years.** In some applications, an existing non-PFAS alternative may be viable, but requires tooling and/or process changes before its successful introduction into high-volume manufacturing. In these cases, it may take between three and 10-plus years to introduce changes to semiconductor manufacturing and related equipment and/or processes, perform qualification testing, and implement the non-PFAS alternative into high-volume manufacturing.
- **Five to 25-plus years – successful invention required.** For some applications, it may not be possible to demonstrate that an available non-PFAS alternative can fulfill the application-specific performance requirements. In those cases, it may be necessary to invent and synthesize new chemicals, and/or develop alternative approaches to fabricating a device structure that provides the necessary electrical and computational performance. Invention is an open-ended endeavor, with no guarantee of success.
- **No alternative achievable.** In some cases, a non-PFAS alternative may not be capable of providing the required chemical function.

13.0 Conclusions

This white paper is part of a comprehensive effort to identify where the semiconductor industry is using PFAS-containing materials, evaluate the application-specific performance requirements, and assess where it is possible to use alternatives.

In wet chemical formulations, a PFAS-containing material may:

- Lower the overall surface tension of the formulation, enabling access to small wafer features (enabling surface tension down to 15 mN/m vs. 30 mN/m).
- Allow wetting and uniform spreading across high-surface-energy materials.
- Provide affinity for certain materials, allowing selectivity between materials (such as CMP) and/or the targeting of certain materials (such as SMT).
- Provide excellent environmental resistance, allowing long shelf life and compatibility with aggressive environments.
- Function under extreme conditions, as provided by low pK_a or other factors.

The requirement to use a particular fluorinated organic chemical depends on the application-specific performance requirements associated with the geometric and material attributes of the device structure being fabricated. Because viability depends on the particular device structure, it is not typically possible to assess a priori whether a PFAS component is essential to conducting a particular wafer fabrication step.

In some applications, there may be opportunities to substitute a non-PFAS component for a currently used PFAS component. For instance, if a formulation already employs both a nonfluorinated and fluorinated surfactant, it is logical to evaluate whether it is possible to use the nonfluorinated surfactant in applications that currently use the fluorinated surfactant. However, given the complexity of semiconductor manufacturing, there is no such thing as a drop-in replacement.

Many fluorinated organic chemical applications used in current wet chemical processing steps have no known alternatives. In some cases, it may be necessary to invent entirely new chemicals. In other cases, an existing chemical may provide a viable alternative.

If an alternative is found, the process of qualification and replacement is a highly complex, multistep, multiyear process. As illustrated in the Substitution Example section, it took eight years to identify, qualify and integrate a shorter-chain PFAS analog for use as an alternative to PFOS in BHF applications. The challenge of finding a nonfluorinated chemical alternative promises to be a far more complex,

resource-intensive and lengthy effort than the comparatively simpler task of substituting to a shorter-chain PFAS analog.

Even incremental changes to semiconductor manufacturing processes require validation through extensive qualification testing to prevent the introduction of unintended consequences into high-volume manufacturing. Once the research and development phase for a new material or process is complete, it typically takes two to five years to qualify and integrate it into an established manufacturing process, as illustrated in Figure 9.

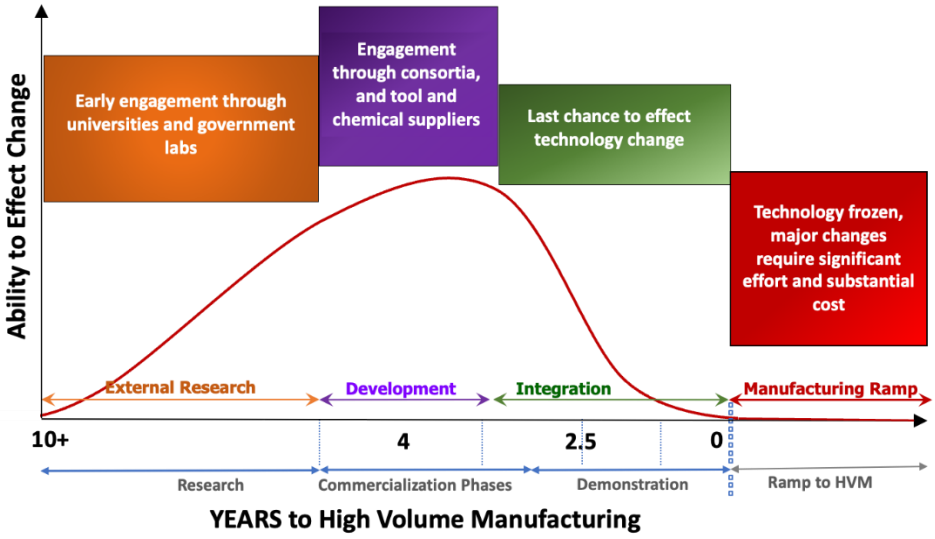

Figure 9: Research and development curve for a large-scale process/technology implementation (Beu 2019).

The major barrier to implementing alternatives lies in the technology cycle of development and the ramp up to high-volume semiconductor manufacturing. Semiconductor manufacturing requires highly integrated manufacturing tools and processes, with hundreds to thousands of interdependent steps that must be conducted at nanometer scales using materials with complex interdependencies. Once a material has been engrained into the semiconductor manufacturing process, it can be excruciatingly difficult to find a viable alternative, prove that the alternative will not disrupt interdependencies, and integrate that alternative into high-volume manufacturing. Historically, the identification of certain failure points only occurred after scaling a process up to higher volumes.

We anticipate that there will be applications where it will not be possible to identify or invent a benign alternative for PFAS. In such instances, it will be necessary to continue using PFAS-containing materials in order to achieve the performance requirements of semiconductor products. In these situations, the use of the PFAS-containing materials must be enabled with controlled and closed systems that mitigate impact to human health and the environment.

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Appendix A: Terminology

The application-specific performance requirements for a process are associated with the particular combination of the device structure-dependent dimensions and materials that are being "operated on," as well as the particular chemical formulation and recipe used in the process. In this context, the need for PFAS-containing materials may depend on the application-specific performance requirements.

This appendix provides more detail about the terms used in this white paper.

Chemical formulation

A "chemical formulation" refers to mixtures of chemicals commonly used to fabricate semiconductors. Examples of chemical formulations are buffered oxide etch, SC1 and SC2.

Recipe

"Recipe" applies to a chemical or chemical formulation in combination with specific equipment parameters. An example of a recipe would be the application of a chemical formulation applied to a wafer at 60°C for 60 seconds.

Process step

"Process step" refers to a series of recipes. There are hundreds of individual process steps, each customized to particular device structures. For example, applications of SC1 and SC2 combined with a water rinse make up a wafer cleaning process step.

Device structure

"Device structure" refers to the individual geometric features of an integrated circuit; for example, transistor gates or contact holes.

Application

An "application" is a specific combination of a chemical formulation and recipe within a process step used to achieve a desired state in a given device structure (Figure A-1).

For example, the use of a chemical formulation to etch a 100-nm diameter contact hole though one material would represent a different application than the use of a chemical formulation to etch a 200-nm contact hole through another material. A PFAS-containing material might be necessary in the chemical formulation for one application but not another, depending on the application-specific performance requirements.

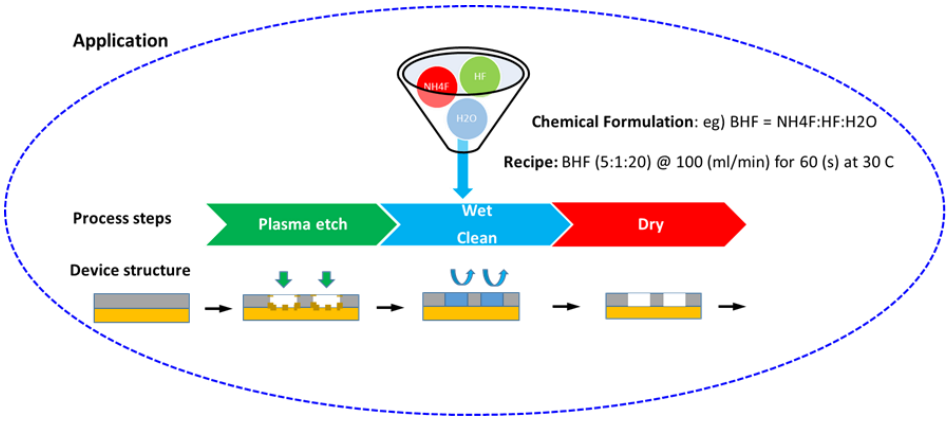

Figure A-1: The term "application" refers to a particular chemical formulation in a specific recipe in a process step to achieve a desired operation on a specific device structure, where the device structure may be associated with a particular product.

Appendix B: Wafer Processing Challenges

The rapid and dramatic evolution in the reduction of the physical scale and geometry of semiconductor devices has an important influence on device fabrication technologies, the performance requirements they must achieve, and therefore the composition of wet chemical formulations. Innovations in chemistry, materials science, manufacturing process technology and device architecture have enabled a 50-year progression in semiconductor technology.

Moore's law characterizes the trajectory of semiconductor technology, whereby the number of transistors in an integrated circuit doubles nearly every two years. Historically, scaling transistor sizes to increasingly smaller physical dimensions, as marked by the technology node, facilitates an increase in transistor density. The technology node is defined in terms of the physical length of the transistor gate, with each new technology node typically representing a 0.7 times reduction in gate length (Khakifirooz, et al. 2012).

In 1984, transistor gate dimensions were on the order of 1 μm, with advanced chips containing more than 1,000 transistors per square centimeter. In 2022, advanced transistor gate dimensions are on the order of just a few nanometers, while advanced chips contain more than 100 million transistors per square centimeter. More recently, the named technology node has not tracked with gate length, with the node name typically much smaller than the actual gate length (Gale 2018); (International Roadmap for Devices and Systems 2022). Transistor density has continued to increase largely through innovations like FinFETs and gate-all-around (GAA) FET nanosheets, which represent a shift from conventional planar architectures to the third dimension.

Planar to 3D Geometry

Planar device architectures were standard until the introduction of FinFETs in the 2010 to 2015 timeframe, where they represent the dominant gate design in 14-, 10- and 7-nm technology nodes. FinFETs were an important architectural innovation that extended the run of gate-length scaling technology nodes by extending gate length into the third dimension (Figure 2). The innovative geometry of these structures introduced new wafer processing challenges, including etch, cleaning, drying and pattern collapse issues (Brown 2022).

It is possible to use GAA FETs with nanosheets in technology nodes beyond 5 nm (Mukesh and Zhang 2022); (International Roadmap for Devices and Systems 2022). GAA FETs cover all sides of a channel while being in contact with the gate (Cho, et al. 2022). The industry is developing stacked nanosheets and GAA structures as a means of improved scaling over what is achievable with FinFETs (Mukesh and Zhang 2022).

Physical dimensions

In addition to the geometric complexity in implementing FinFETs and GAA FETs, the physical dimensions of the features that must undergo wet chemical processing will continue to reach new extremes. At the 7-nm technology node, for instance, dummy gates may be only 8-nm wide, and the holes between fins may be 4-nm-by-8-nm wide and 60-nm deep (Vereecke, De Coster, et al. 2018). Deep contact holes in 3D NAND memory may have aspect ratios of 60 or higher (Cho, et al. 2022).

Processing challenges

3D NAND-type flash memory is common in solid-state hard drives and USB storage devices, where it provides high memory density, lower energy consumption and faster writing performance in comparison to conventional 2D NAND (Zhou, et al. 2023). In the drive for improved memory density and

performance, the number of stacked layers has increased to over 200 (Park, et al. 2023); (Zhou, et al. 2023).

Vertical NAND cells are fabricated from stacked silicon nitride/silicon dioxide layers by a CVD process, followed by the vertical punching of through-holes by dry etching and the selective removal of silicon nitride by wet chemical etching, as illustrated in Figure 3. The challenges in wet etching a silicon nitride/silicon dioxide paired-layer 3D NAND multistack structure are representative of the continuing innovations required of aqueous etch formulations. The extreme aspect ratio and materials selectivity challenges require continuing innovation in the development and use of additives to supplement the action of an acidic or basic etchants.

More generally, there are a number of fundamental physicochemical concerns that challenge the extendibility of traditional wet etch processes into such narrowly dimensioned, high-aspect-ratio geometric features (Vereecke, De Coster, et al. 2018). For instance, in low-nanometer dimension channels, the electrostatic double layer that exists at walls affects charge and ion distribution and extends well into the channel width. It is not clear how increasingly small dimensions will affect the mass transport, mass transfer and concentration distribution of both reactants and reaction products (Vereecke, De Coster, et al. 2018). Early reports indicate that in deep nanoscale trenches, the wetting of water and even water-ethanol mixtures can be incomplete, and affected by the formation of nanobubbles (Vereecke, Darcos, et al. 2021); (Vereecke, Kenis, et al. 2022). Evidence of the structuring of water molecules has been reported even in 20-nm diameter nanoholes (Vereecke, Kenis, et al. 2022).

